CMSC 311 Midterm #2 - Fall 1994

Name ________________________________ Signature ________________________________

(1) This exam is closed book, closed notes, and closed neighbor.

(2) You have 70 minutes to complete this exam. If you finish early, you may turn in your exam at the front of the room and leave. However if you finish during the last ten minutes of the exam please remain seated until the end of the exam so you don't disturb others.

(3) Write all answers on the exam. If you need additional paper, I will provide it. Make sure your name is on any additional sheets.

(4) Partial credit will be given for most questions assuming I can figure out what you were doing.

(6) Please write neatly. Print your answers if your handwriting is hard to read. If you write something, and wish to cross it out, simply put an X through it. Please indicate if your answer continues onto another page.

(7) When showing multiple lines connected between the same two components, use a single line to represent all lines.

Question	Possible	Score
1	20	
2	15	
3	15	
4	25	
5	25	
Total	100	

Name of the person Sitting to your

left ________________________________ right ________________________________

1.) (20 points) Define the following terms:

a.) Three-state Gate (tri-state buffer)

b.) Gray code

c.) Micro-instruction

d.) Binary Coded Decimal

e.) Stored Program Computer

2.) (15 points) Convert the following decimal numbers to the requested format.

a.) Fill the following table the binary representation of the numbers in each row in requested format for each column.

Number	8 bit Signed-magnitude	8 bit 1's complement	8 bit 2's complement
-0			
-1			
-15			
100			

b.) Represent the number $(+45.125)_{10}$ as a floating-point binary number with 24 bits. The normalized fraction mantissa has 16 bits and the exponent has 8 bits.

3.) (15 points) Design a 9-bit odd parity generator using four 3-bit odd parity generators and at most one additional logic gate of any type (with 2 or fewer inputs). Draw a diagram showing your design. Be sure to label all of the inputs and outputs of the 3-bit generators and of the 9-bit generator.

4.) (25 points) In class we talked about hardware for addition and subtraction. This question deals with how to perform multiplication. One way to multiply two numbers is to use repeated addition. For example (3 * 4 = 3 + 3 + 3 + 3).

a) When multiplying an n-bit unsigned number by an m-bit unsigned number, what is the maximum number of bits required for the product?

b) Design a 4 bit (unsigned) multiplier using a 4 bit count down counter with load, 2 four bit registers, a four bit adder, one D Flip-flop, and logic gates. Your circuit should have two four bit inputs for the operands and a control line (LOAD) to indicate the operands are present. The output should be one four bit number, a one bit overflow indicator, and a one bit signal (READY) to indicate the multiplication is done.

c) What is the maximum number of clock pulses required to multiply any two numbers with your circuit?

5.) (25 points) To improve the ability of Mano's basic computer to handle large numbers, you have been given the task of updating the computer to handle 32 bit arithmetic (by making the AC, DR, and ALU 32 bits wide). However, to remain compatible with previous models, all other registers, the memory, and the system bus are to remain the same size (12 or 16 bits). As a result, only half of the AC or DR registers can be on the bus at once. The register transfer language (RTL) has been augmented to describe which word (high or low) of the AC or DR should be used. For example, to copy the AR to the low half of the AC, the RTL would be:

low(AC) <- AR

a) Design the new AC register using two copies of the old AC, and logic gates. In addition to 32 data input and 16 data output lines, it should have control lines for LOAD, INC, CLR, and a line to select which word of the register should be the output.

b) Write the RTL to load the DR with a 32 bit value in the extended Mano machine. The value contained in the temporary register (TR) is the address of the lower of two consecutive memory locations that should be loaded into the low and high halves of DR respectively.

c) Give two reasons why this extended 16 bit machine is not as capable or efficient as a new machine with **all** registers, memory, and the bus 32 bits wide.