CMSC 311- Computer Organization

Fall 1995 - Assignment #7 (solution)

1)

XOR	D_0T_4:	$DR \leftarrow M[AR]$
	D_0T_5:	$AC \leftarrow AC\ (+)\ DR,\ SC \leftarrow 0$
ADM	D_1T_4:	$DR \leftarrow M[AR]$
	D_1T_5:	$DR \leftarrow AC,\ AC \leftarrow AC + DR$
SUB	D_2T_4:	$DR \leftarrow M[AR]$
	D_2T_5:	$DR \leftarrow AC,\ AC \leftarrow AC + DR$
	D_2T_6:	$AC \leftarrow AC'$
	D_2T_7:	$AC \leftarrow AC + 1$
	D_2T_8:	$AC \leftarrow AC + DR,\ SC \leftarrow 0$
XCH	D_3T_4:	$DR \leftarrow M[AR]$
	D_3T_5:	$M[AR] \leftarrow AC,\ AC \leftarrow DR,\ SC \leftarrow 0$
SEQ	D_4T_4:	$DR \leftarrow M[AR]$
	D_4T_5:	$TR \leftarrow AC,\ AC \leftarrow AC\ (+)\ DR$
	D_4T_5:	if $(AC = 0)$ then $PC \leftarrow PC + 1,\ AC \leftarrow TR,\ SC \leftarrow 0$
BPA	D_5T_4:	if $(AC\ != 0\ \wedge\ AC(15) = 0)$ then $PC \leftarrow AR,\ SC \leftarrow 0$

2)

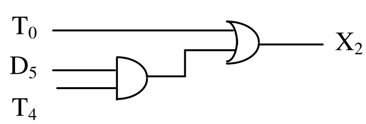
X_2 places PC onto the bus. From table 5-6:

$R'T_0$: $AR \leftarrow PC$

$R\ T_0$: $TR \leftarrow PC$

D_5T_4: $M[AR] \leftarrow PC$

$$X_2 = R'\ T_0 + R\ T_0 + D_5T_4 = T_0 + D_5T_4$$



3)

a) $PC = 01011_{16}$, $AC = 5555_{16}$, $AR=100_{16}$, $R = 0$

b) No.

c) $PC = 0101_{16}$, $AC = 0000_{16}$, $AR = 200_{16}$, $IR = 0200_{16}$, $R = 0$

4)

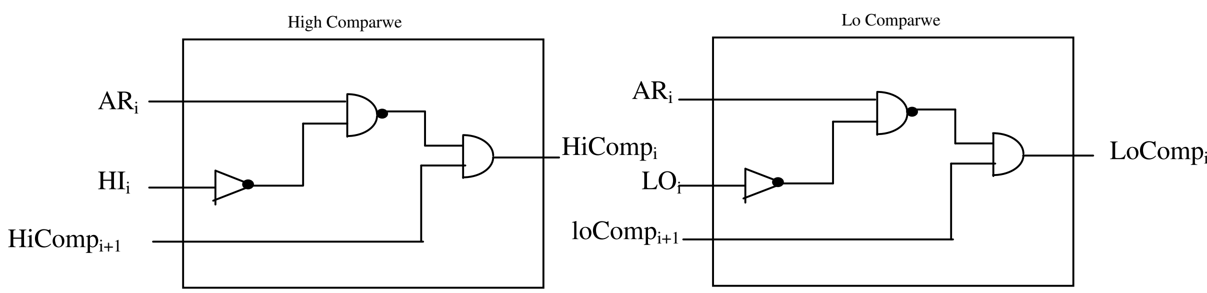
a) SLO $D_7IT_3B_5$: LO $\leftarrow$ AC, SC $\leftarrow$ 0

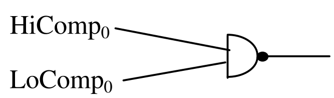
SHI $D_7IT_3B_4$: HI $\leftarrow$ AC, SC $\leftarrow$ 0

b) Consider 1 bit A <= B function and on bit A >= B function

AB	A<= B	A>= B
00	1	1
01	1	0
10	0	1
11	1	1

For A <= B, in the I^{th} bit position, the output should be a 1 if the output of the I + 1 bit position is a 1 and A_i <= B_i





c) Let Z represent the trap cycle (i.e. its a flip-flop like R is for interrupt). Invalid is the output of part b, we attach the inputs to the LO and HI registers, and the bus. The idea is to prevent any part of the instruction from executing after it tries to refer to an invalid memory reference. We also add Z' before all other non-trap cycle instructions. We change the normal fetch and decode to be:

$Z'R'T_0$: AR $\leftarrow$ PC, Z $\leftarrow$ Invalid, TR $\leftarrow$ PC
$Z'R'T_1$: IR $\leftarrow$ M[AR], PC $\leftarrow$ PC + 1
$Z'R'T_2$: normal decode, Z $\leftarrow$ Invalid ^ D'_7
$Z'D'_7IT_3$: AR $\leftarrow$ M[AR], Z $\leftarrow$ Invalid

For the trap cycle,

ZT_0: AR $\leftarrow$ 0
ZT_1: AR $\leftarrow$ AR + 1
ZT_2: AR $\leftarrow$ AR + 1
ZT_3: M[AR] $\leftarrow$ TR, AR $\leftarrow$ AR + 1
ZT_4: PC $\leftarrow$ AR, AC $\leftarrow$ 0, Z $\leftarrow$ 0

5)

```
        LDA   A
        SZA
        BUN NZR
        HLT
NZR,    CMA
        INC
        STA CTR
        CLA
LOP,    ADD B
        ISZ CTR
        BUN LOP
        HLT
A,      DEC 0
B,      DEC 0
CTR,    HEX 0
        END
```