Question 1: Amdahl's Law

$$Speedup_{Overall} = \frac{Exec.Time_{Old}}{Exec.Time_{New}} = \frac{1}{(1 - fraction_{enhanced}) + \frac{fraction_{enhanced}}{speedup_{enhanced}}}.$$

a. $Speedup_{Overall} = 1.7$

$speedup_{enhanced} = x$

$$1.7 = \frac{1}{(1 - fraction_{enhanced}) + \frac{fraction_{enhanced}}{x}}.$$

$$1.7 = \frac{x}{x - x * fraction_{enhanced} + fraction_{enhanced}}.$$

$1.7x - 1.7x * fraction_{enhanced} + 1.7 * fraction_{enhanced} = x$

$- 17x * fraction_{enhanced} + 1.7 * fraction_{enhanced} = x - 1.7x$

$$- x * fraction_{enhanced} + fraction_{enhanced} = \frac{x - 1.7x}{1.7}$$

$$fraction_{enhanced} = \frac{x - 1.7x}{1.7(1 - x)}.$$

b.

$fraction_{enhanced} = 0.50$

$Speedup_{Overall} = 1.25$

$speedup_{enhanced} = x$

$$1.25 = \frac{1}{(1 - 0.5) + \frac{0.50}{}}.$$

$$1.25 = \frac{x}{0.50x + 0.50}$$

$$x = \frac{1.25(0.50)}{1 - 1.25(0.50)}$$

$$x = 1.667$$

Question 2:CPI

Information Given:

Perfect Cache:

Type	Frequency	Number of Clock Cycles
ALU Operations	30%	1
Loads	30%	2
Stores	20%	2
Branches	20%	2

Imperfect Cache

Instruction Fetch Miss Rate = 5%

Load/Store Miss Rate = 90%

Miss Penalty = 40 clock cycles

(a) CPI for Each Instruction Type:

$CPI = CPI_{Perfect} + CPI_{Stall}$

$CPI = CPI_{Perfect} + (Miss\ Rate * Miss\ Penalty)$

$CPI_{ALUops} = 1 + (0.05 * 40) = 3$

$CPI_{Loads} = 2 + [(0.05 + 0.90) * 40] = 40$

$CPI_{Stores} = 2 + [(0.05 + 0.90) * 40] = 40$

$CPI_{Branches} = 2 + (0.05 * 40) = 4$

(b) CPI for the Overall Machine:

$$CPI_{Overall} = \sum_{i=1}^{4} CPI_i * IC_i / IC_{total}$$

$$CPI_{Overall} = \sum_{i=1}^{4} CPI_i * (\text{Relative Frequency})$$

$CPI_{Overall} = (CPI_{ALUops} * 0.30) + (CPI_{Laod} * 0.30) + (CPI_{store} * 0.20) + (CPI_{branch} * 0.20)$

$CPI_{Overall} = (3 * 0.30) + (40 * 0.30) + (40 * 0.20) + (4 * 0.20)$

$CPI_{Overall} = 21.70$

(c) Speed of Machine with NO Cache Misses

$$CPI_{perfect} = \sum_{i=1}^{4} (CPI_{i\ perfect} * \text{Relative Frequency})$$

$CPI_{perfect} = 1 * 0.30 + 2 * 0.30 + 2 * 0.20 + 2 * 0.20$

$CPI_{perfect} = 1.7$

$$Speedup_{with\ perfect\ cache} = \frac{Exec.Time_{Overall}}{Exec.Time_{perfect}} = \frac{IC * CPI_{Overall} * CCT}{IC * CPI_{perfect} * CCT}$$

$$Speedup_{with\ perfect\ cache} = \frac{IC * 21.7 * CCT}{IC * 1.7 * CCT} = 12.76$$

Question 3:Tradeoffs

Information Given:

A Tradeoff takes place between the Instruction Count (IC) and the Cycles per Instruction (CPI).
Decreasing the number of Instructions increase the CPI since 1-2 clock cycles are added per instruction.

$CPI_{perfect}$ = 1.7 from previous question

$CPI_{ALUops} = 0.20(1) + 0.15(2) + 0.10(1) + 1 = 1.6$ cycles

$CPI_{Load} = 2$ cycles

$CPI_{Store} = 2$ cycles

$CPI_{Branches} = (2 + n)$ cycles

$IC_{ALUops} = 0.30$

$IC_{Load} = 0.30 - 0.30(0.20)(1) - 0.30(0.15)(2) = 0.15$

$IC_{Stores} = 0.20 - 0.30(0.10)(1) = 0.17$

$IC_{Branches} = 0.20$

a. Must find **n = max. tolerable increase in clock cycle count for the branche**s—yielding a design that performs better than the new one

$CPU_{Perfect} = CPU_{tradeoff}$

$1.70*(IC_{Total}) = (CPI_{ALU\ opS} * IC_{ALU\ opS}) + (CPI_{LoadS}*IC_{LoadS}) + (CPI_{StoreS}*IC_{StoreS}) + (CPI_{BrancheS}*IC_{BrancheS})$

$1.70*(IC_{Total}) = [(0.30*1.6) + (0.15*2) + (0.17*2) + (0.20*\{2 + n\})][\ IC_{Total}]$

$n = 0.9$

b. Must determine **x = max. tolerable percent increase in clock cycle time**—yielding a design which performs better than the original design

$CPU_{Exec\ Time\ Old} = CPU_{Exec\ Time\ New}$

$1.7*(IC_{Total\ Clock\ Cycle}) = (CPI_{ALU\ ops}*IC_{ALU\ ops}) + (CPI_{Loads}*IC_{Loads}) + (CPI_{Stores}*IC_{Stores}) + (CPI_{Branches}*IC_{Branches})$

$1.7*(IC_{Total}) = [(0.30*1.6) + (0.15*2) + (0.17*2) + (0.2*2)][\ IC_{Total}\ ]\ ][1 + x]$

$x = 11.84\%$

Question 4: More Tradeoffs

PART (a)

Ideal Machine:

$CPU_{Execution\ Time} = (CPU_{Clock\ Cycles} + \text{Memory Stall Cycles}) \times \text{Clock Cycle}$

$= (IC \times CPI + 0) \times \text{Clock Cycle}$

$= IC \times 2 \times \text{Clock Cycle}$

Memory Stall Cycles = IC x Memory References per Instruction x Miss Rate x Miss Penalty

Memory Stall Cycles = IC x (1 x 0.025 x 40 + 0.4 x 0.01 x 40)

$= IC \times 1.16$

$CPU_{Execution\ Time\ (Cache)} = (CPU_{Clock\ Cycles} + \text{Memory Stall Cycles}) \times \text{Clock Cycle}$

$= (IC \times [2 + 1.16]) \times \text{Clock Cycle}$

$= IC \times 3.16 \times \text{Clock Cycle}$

Performance Ratio*:*

$$\text{Performance Ratio} = \frac{CPU_{Execution\ Time\ (Cache)}}{CPU_{Execution\ Time}} = \frac{3.16}{2} = 1.58$$

PART (b)

Number of Non Loads/Stores: $IC_{old} \times 0.6$

Number of Loads/Stores: $IC_{old} \times 0.4(1-0.3) = 0.28IC_{old}$

Total # of $IC_{New} = 0.88 \times IC_{Old}$

Memory Stall Cycles = Instruction Misses + Data Misses = [IC_{New} x Instruction Miss Rate x Instruction Miss Penalty] +

[Number of Loads/Stores x Data Miss Rate x Data Miss Penalty]

$= IC_{Old} \times 0.88 \text{ X } 0.025 \times 40 + IC_{Old} \times 0.28 \times 0.01 \times 40$

$= 0.88 \times IC_{old} + 0.112 \times IC_{old}$

$= 0.992 \times IC_{Old}$

$CPU_{Execution\ Time} = (0.88*2*IC_{Old} + 0.992*IC_{Old}) CC_{Old} * 1.05$

$= IC_{Old} * 2.8896 * CC_{Old}$

$$\text{Speedup} = \frac{CPU_{Execution\ Time\ Old}}{CPU_{Execution\ Time\ New}} = \frac{IC_{Old} * 3.16 * CC_{Old}}{IC_{Old} * 2.8896 * CC_{Old}} = 1.094$$