Suppose that we have implemented a (0,3) GPR machine, using a Superscalar Speculative Tomasulo (SST) architecture that executes the MIPS ISA. For each of the questions in this section, write the letter T next to the statements below that are True, and briefly explain why the others are false.

1.1 The SST uses static scheduling to maximize the amount of ILP that can be exploited at execution time.
   False: uses dynamic scheduling

1.2 An instruction will remain in the reorder buffer of the SST until all instructions issued during the same clock cycle have committed.
   False: stays in reorder buffer until at the top and committed, or if speculated incorrectly, will be flushed.

1.3 The Ideal CPI of the SST is less than 1.
   True: superscalar goal is CPI; 1

1.4 The SST compiler uses a branch delay slot to deal with control hazards.
   False: branch delay slot is static handling of control hazards; speculative requires dynamic prediction.

1.5 Speculative execution permits the SST to issue several instructions in a single clock cycle.
   False: superscalar permits several instructions to be issued in a single clock cycle, Speculative execution means that you predicted (prior to confirmation) the direction to be taken by a branch, and executed some instructions based on that speculation, At best, if you predicted correctly, you have no (or minimal) stalls because you kept executing along a correct path while the branch was being decided,
   At worst, you have to flush all the incorrectly executed instructions, called “speculated instructions”, and then execute the correct ones, however, the experienced branch penalty should still be no more than the time needed to evaluate the branch condition and start the correct next instruction (in the absence of memory delays, of course, but that’s another issue)
Problem 2: What’s My Line? (16 pts)

Now, we turn to control hazards, and see what you’ve learned to protect yourself from them. As with the previous quiz, the correct answer(s) come the set of terms below. For each statement, identify the “speaker” by writing the Letter(s) corresponding to the term(s) for which the statement is true.

Potential Answers:
D (branch Delay slots)
P (branch Folding)
P (branch Prediction buffer)
T (branch Target buffer without prediction)
All (All of the above)
None (None of the above)
Other (fill in your Own answer)

1. I am a dynamic method to decrease the stalls caused by control hazards. (All but D.)
2. I am a static method to decrease the stalls caused by control hazards. (D)
3. I eliminate all stalls due to control hazards. (N)
4. I may consult a 2-bit saturating predictor. (P)
5. I contain the the next instruction to be executed after a known unconditional branch instruction. (F)
6. If a branch was just taken, I will predict “taken” the next time that the specific branch is fetched. (N)
7. I am a cache that tracks branching history for every known branch in the program. (T)
8. I contain the expected next PC value after the branch condition has been evaluated. (N. It’s only “T” if the branch is taken,)