
CMSC 411
Computer Systems Architecture
Project
Cache Simulator

Simulation Approach

- Trace-driven
 - Sequence of memory accesses
 - » Taken from actual execution on machine
- Cache model
 - Maintain cache in software
- Software
 - C code
 - Text files listing application traces
 - » spice, cc, tex

Simulation Statistics

- Number of instruction references
- Number of data references
- Number of instruction misses
- Number of data misses
- Number of words fetched from memory
- Number of words copied back to memory

Cache Simulator

- Goals
 - Build a cache simulator
 - Validate correctness
 - Use cache simulator to study
 - » Cache organizations
 - » Cache management policies

Cache Parameters

- Total cache size
- Block size
- Unified vs. split I- and D-caches
- Associativity
- Write back vs. write through
- Write allocate vs. write no allocate

Project Milestones

1. Basic cache
 - 8K direct mapped, unified cache
 - Block size = 16, write back, write allocate
2. Vary cache parameters
 - Size, associativity, etc...
3. Performance evaluation
 - Working set
 - Impact of
 - » Block size
 - » Associativity
 - » Memory bandwidth (writeback vs writethrough, etc.)