

CMSC 411 Practice Exam 1

General instructions.

Be complete, yet concise. You may leave arithmetic expressions in any form that a calculator could evaluate.

1. CPU performance

Suppose we have the following instruction mix and clock cycles per instruction.

Instruction	Frequency	Cycles
ALU operations	30%	1
Load	20%	2
Store	10%	2
Branches	20%	3
Floating point operations	20%	5

- What is the overall CPI of this machine?
- If the CPU runs at 750MHz, what is the MIPS rating of this machine? For this question, count floating point operations in the MIPS rating.
- Consider improving this computer's performance by enhancing the speed of the floating point instructions. What is the best possible overall speedup that we could obtain?

2. Speedup

Two enhancements, E_1 and E_2 , with the following speedups are proposed for a new architecture:

$$\text{Speedup}_1 = 10$$

$$\text{Speedup}_2 = 5$$

Only one of the enhancements is usable at any point in time (maybe because they use some of the same hardware).

- (a) If E_1 can be used 20% of the time and E_2 can be used 10% of the time, what would be the overall speedup?
- (b) If the percentage of time that E_1 can be used decreased to 15%, what percentage of the time would the use of E_2 have to be to get the same overall speedup as in part (a)?
- (c) Suppose we are free to choose between E_1 or E_2 , whenever we want (the percentages of time for using E_1 or E_2 can be varied as desired, but in total cannot be more than 100% of the time). What would be the maximum achievable overall speedup?

3. MIPS ISA

- (a) Suppose that a is stored in memory location 10, b is stored in memory location 20, and c is stored in memory location 30. Assume that all three variables are double word integers. Write MIPS assembly code equivalent to the following C code fragment:

```
a = 4;  
c = a + b;
```

Don't worry about the exact syntax of the MIPS instructions (but get the addressing mode right). However, you must make your intent for each instruction clear. Remember that there is no load immediate MIPS instruction, to put a constant in a register.

- (b) Give 2 reasons why the MIPS architecture can get away with only 2 addressing modes, immediate and displacement.

4. Basic pipelining

Consider the following MIPS code:

```
I1: DADD R1, R5, R3
I2: DADD R3, R1, R5
I3: SD    R5, 10(R1)
I4: DADD R5, R1, R3
```

Suppose we have the simple MIPS 5-stage pipeline from Appendix A in the book (and every instruction must go through all 5 stages).

- (a) Fill in the first pipeline table showing execution of the instructions assuming that no forwarding is available, then fill out the second table assuming that forwarding is available in the pipeline wherever it is needed.

Without forwarding

	1	2	3	4	5	6	7	8	9	10	11	12	13
I1	IF	ID	EX	MEM	WB								
I2													
I3													
I4													

With forwarding

	1	2	3	4	5	6	7	8	9	10	11	12	13
I1	IF	ID	EX	MEM	WB								
I2													
I3													
I4													

- (b) Show and classify all the potential data hazards (RAW, WAR, WAW). Which of the potential RAW data hazards are eliminated because of forwarding?