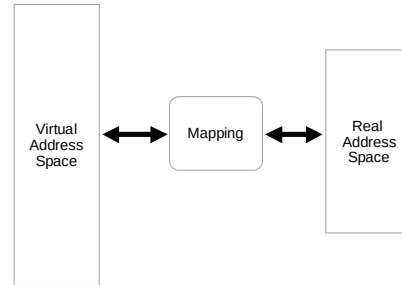
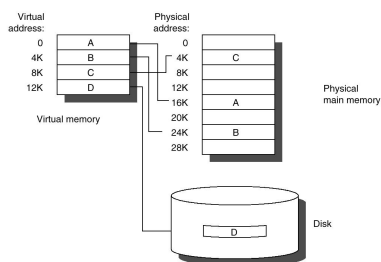


Memory Hierarchy and Cache Design (4)

Virtual vs Real Address Spaces



Virtual Memory - the logical concept



Virtual Memory vs Cache

Parameter	First-level cache	Virtual memory
Block (page) size	16–128 bytes	4096–65,536 bytes
Hit time	1–2 clock cycles	40–100 clock cycles
Miss penalty	8–100 clock cycles	700,000–6,000,000 clock cycles
(Access time)	(6–60 clock cycles)	(500,000–4,000,000 clock cycles)
(Transfer time)	(2–40 clock cycles)	(200,000–2,000,000 clock cycles)
Miss rate	0.5–10%	0.00001– 0.001%
Data memory size	0.016–1MB	16–8192 MB

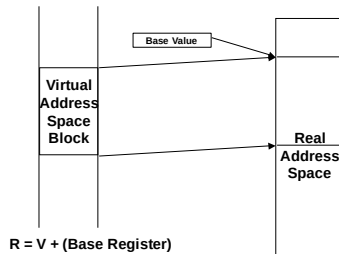
Virtual Memory vs Cache

- **Replacement**
 - Cache - controlled by hardware
 - Virtual memory - controlled by operating system
 - » HUGE miss penalty
- **Size**
 - Virtual memory size is determined by processor address size
 - Cache size is independent of processor address size
- **Combined usage of secondary memory**
 - Backing store of main memory
 - File system

Types of Virtual Memory

- **Paged**
 - Fixed size blocks (pages)
 - Size usually 4K-64Kbytes
- **Segmented**
 - Variable size blocks
 - Sizes vary

Mapping

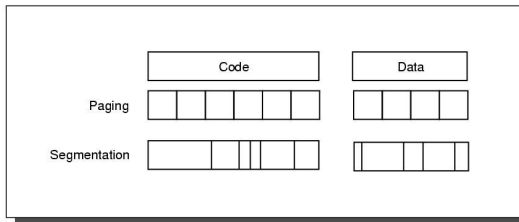


Mapping requires one Base Value for each block
Blocks may be of same size or varying size

Segmentation and Paging

- **Segmentation**
 - Organize Virtual Address Space in variable size blocks
 - Need information about the length of blocks also
 - Addresses from one segment to the next may not be considered contiguous
 - Virtual address
 - » {Segment ID, Offset in Segment}
- **Paging**
 - Organize Virtual Address Space in fixed size blocks
 - Virtual Address
 - » {Single Address}

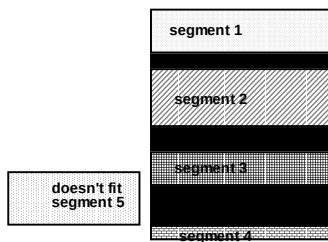
Segmentation vs Paging



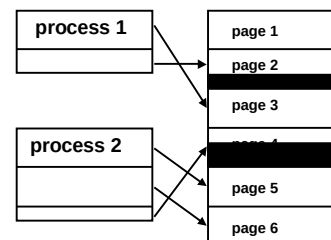
Segmentation vs Paging

	Page	Segment
Words per address	One	Two (segment and offset)
Programmer visible?	Invisible to application programmer	May be visible to application programmer
Replacing a block	Trivial (all blocks are the same size)	Hard (must find contiguous, variable-size, unused portion of main memory)
Memory use inefficiency	Internal fragmentation (unused portion of page)	External fragmentation (unused pieces of main memory)
Efficient disk traffic	Yes (adjust page size to balance access time and transfer time)	Not always (small segments may transfer just a few bytes)

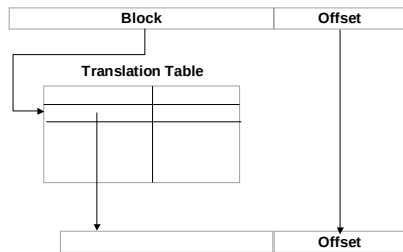
External Fragmentation



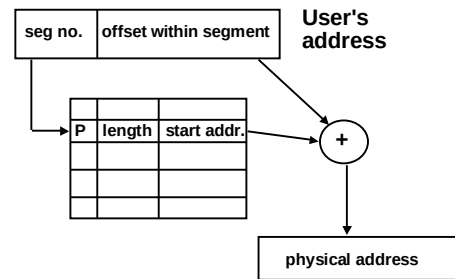
Internal Fragmentation



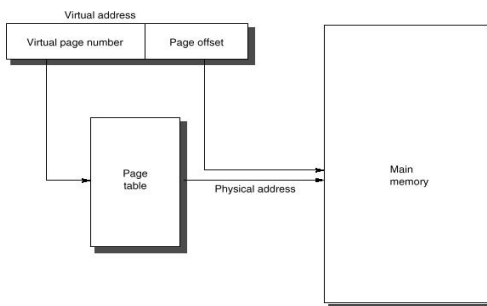
Translating Virtual Addresses



Segmentation



Paging Address Translation



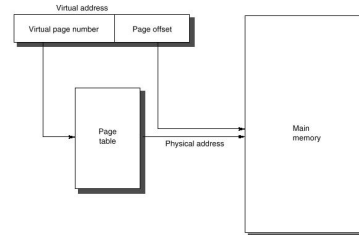
Four Questions for Virtual Memory

- Block Placement: Fully Associative
- Block Identification: Fully Associative
- Block Replacement: LRU or its variants
- Write Strategy: Write back & Write allocate

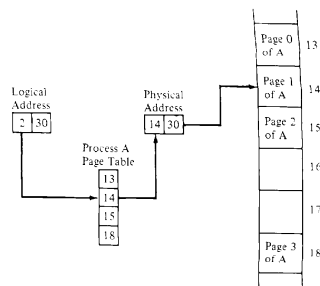
Block Placement

- **Fully Associative** - the obvious choice
 - Huge miss penalty - low miss rate is extremely important
 - VM managed by software in OS - much more flexible than cache managed by hardware

Block Identification

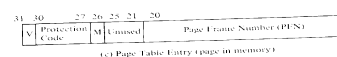
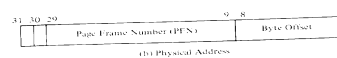
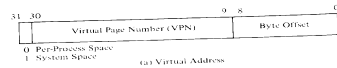


Paging Logical to Physical Addresses

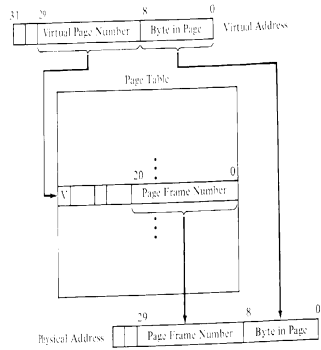


VAX Memory Management

- **32 Bit addresses**
- **4 GB Virtual Address Space**
- **512 Bytes per page** 2^{23} pages
- **Real Address Space is limited to 1GB**



Address Translation



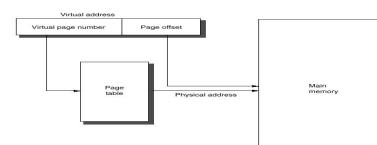
Block Replacement

- Pure LRU is difficult, if not impossible, to implement
- The Clock Algorithm
 - Maintain a circular list of pages in physical memory
 - » Use a *use* bit to track how recently a page is referenced
 - » Use bit set whenever a page is referenced
 - On a page fault, look for a page with *use* bit = 0 (in the clock order)
 - » Replaces a page that hasn't been referenced for one complete revolution of the clock

Write Strategy

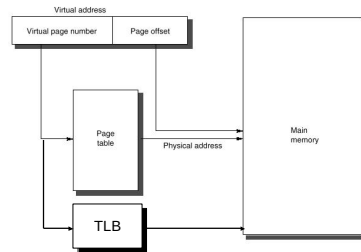
- Write back - the obvious choice

Fast Address Translation

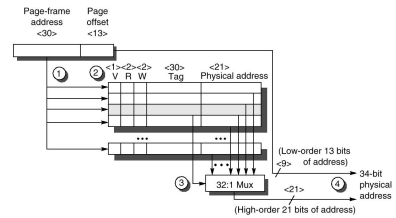


- Page tables are large and often paged
- Need fast mechanism for address translation
- USE
 - TRANSLATION LOOK-ASIDE BUFFERS (TLB)
 - Associative memory

TLB: Page Table Cache



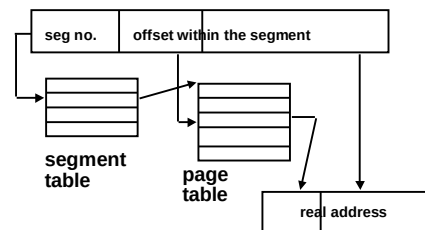
More Details on TLB (Alpha AXP 21064 TLB)



Page Size

- Size of page table is inversely proportional to the page size
- Transferring larger pages to and from the secondary storage is more efficient than smaller pages
- As TLB sizes are restricted, larger page sizes imply more address space can be translated
- Larger page sizes lead to higher internal fragmentation
- Larger pages lead to higher startup time for a process

Segmentation and Paging



Segmentation and Paging

	Segmentation	Paging
1. Block size	Variable	Fixed
2. Placement	First fit, et al.	Fully associative
3. How found	Size+location	Page table registers
4. Replacement	by programmer	LRU
5. Write action	Write back	Write back
Fragmentation	External	Internal
Programming	Visible	Transparent
Protection	RO, RW, EX	Difficult

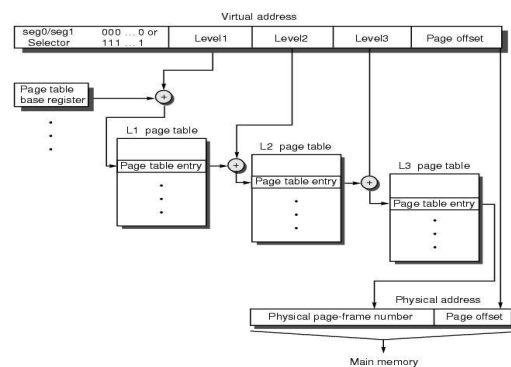
Protection

- Have bounds register and check it for each access
 - Have at least two modes - *Kernel and User*
 - Have CPU states that can be used by a user but not modified - Base and Bound Registers ...
 - Controlled change of mode - System Call

Example - AXP 21064

- 64-bit addresses
 - kseg - (bits 63 and 62 = 10)
 - » Reserved for Operating system kernel
 - » Uses no memory management
 - » Uniform protection
 - Seg0 - Bit 63 = 0
 - seg 1 - (bits 63 and 62 = 11)
 - User processes use Seg 0 and Seg1
 - » Mapped to pages with individual protection
 - » Seg0 grows upwards and Seg 1 downwards
- Three level hierarchical page table

Mapping of an Alpha Virtual Address



- 8KB pages
- Entries are 64 bit (8 bytes) long
 - 32 bit contain physical page frame number
 - 5 protection Fields
 - » Valid
 - » User read enable
 - » Kernel read enable
 - » User write enable
 - » Kernel write enable
 - Fields reserved for system software use
 - One page contains 1024 PTEs
 - Each Level is 10 bits long
 - Leaves 21 bits to be defined!!!
 - » For Seg0 all are 0 and for Seg1 all are 1
- Virtual addresses are 43 bits long and not 64
- Physical address are 34 bits, not 32+13
 - Requirement: physical address < virtual address

Alpha Page Table

Address Spaces

- Influenced by page size
- E.g. Page Size: 64 KB
- Virtual address - $3 \times 13 + 16 = 55$ bits
- Physical address - $32 + 16$ or 48 bits

Memory Hierarchy TLB Parameters

Use two TLBs - One for instructions and one for data
OS can tell TLB to treat contiguous sequences of pages as one

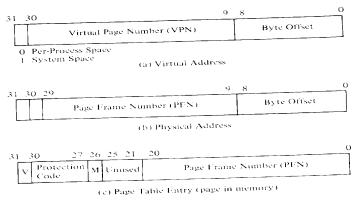
- Block Size 1 PTE (8Bytes)
- Hit Time 1 clock cycle
- Miss Penalty(Avg) 20 cycles
- TLB Size
 - Instruction: 8PTE for 8KB pages
 - 4 PTE for 4 MB pages
 - (96 bytes total)
 - Data: 32 PTE for 8-KB, 64 KB, 512KB, 4 MB
 - (256 Bytes total)
- Block Selection Random, but not last used
- Write Strategy (Not Applicable)
- Block Placement Fully Associative

**Overall
Picture -
AXP 21064**

Copyright 1995, 1996, 1997, 1998, 1999, 2000, 2001, 2002, 2003, 2004, 2005, 2006, 2007, 2008, 2009, 2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017, 2018, 2019, 2020, 2021, 2022, 2023, 2024, 2025, 2026, 2027, 2028, 2029, 2030, 2031, 2032, 2033, 2034, 2035, 2036, 2037, 2038, 2039, 2040, 2041, 2042, 2043, 2044, 2045, 2046, 2047, 2048, 2049, 2050, 2051, 2052, 2053, 2054, 2055, 2056, 2057, 2058, 2059, 2060, 2061, 2062, 2063, 2064, 2065, 2066, 2067, 2068, 2069, 2070, 2071, 2072, 2073, 2074, 2075, 2076, 2077, 2078, 2079, 2080, 2081, 2082, 2083, 2084, 2085, 2086, 2087, 2088, 2089, 2090, 2091, 2092, 2093, 2094, 2095, 2096, 2097, 2098, 2099, 2100, 2101, 2102, 2103, 2104, 2105, 2106, 2107, 2108, 2109, 2110, 2111, 2112, 2113, 2114, 2115, 2116, 2117, 2118, 2119, 2120, 2121, 2122, 2123, 2124, 2125, 2126, 2127, 2128, 2129, 2130, 2131, 2132, 2133, 2134, 2135, 2136, 2137, 2138, 2139, 2140, 2141, 2142, 2143, 2144, 2145, 2146, 2147, 2148, 2149, 2150, 2151, 2152, 2153, 2154, 2155, 2156, 2157, 2158, 2159, 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VAX Memory Management

- 32 Bit addresses
- 4 GB Virtual Address Space
- 512 Bytes per page 2^{23} pages
- Real Address Space is limited to 1GB

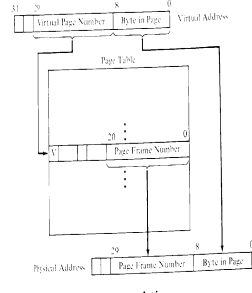


Access Control

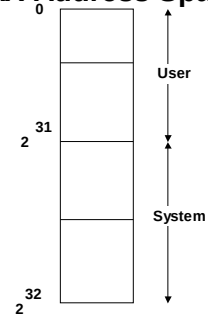
- Access Level
 - No Access
 - Read Only Access
 - Read/Write Access
- Access Mode
 - Kernel
 - Kernel functions of the OS
 - Executive
 - System Calls
 - Supervisor
 - Operating system services e.g. responses to user commands
 - User

Each page in memory is defined to have a particular access level for each access mode

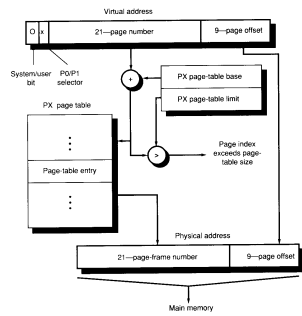
Address Translation



VAX Address Space



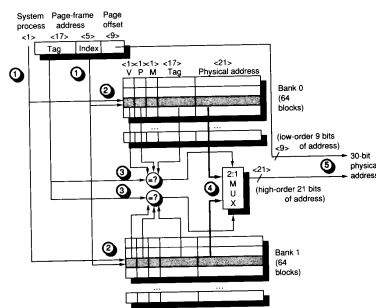
VAX Address Translation



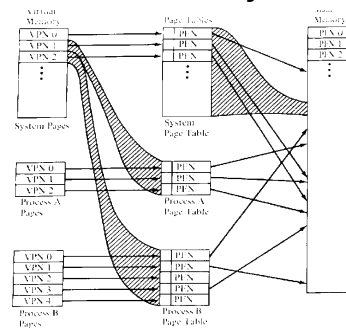
VAX TLB

- 2 Way Set Associative
- 64 entries per set
 - Divided into 32 entries for system and 32 for process

VAX TLB



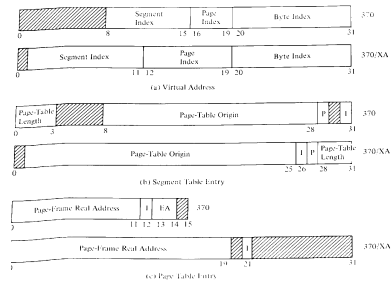
VAX Virtual Memory Scheme



System/370 Memory Management

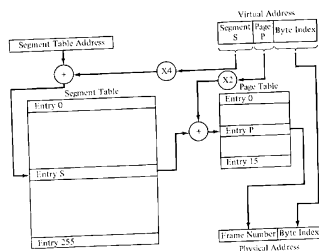
- Two level
 - Segments
 - Pages
- Page size
 - 2KB or 4KB
- Segment Size
 - 64KB or 1MB
- For 370/XA 4KB pages and 1M segments

Address Formats



Structure

- One segment table for each virtual address space
- One page table for each segment



INTEL 80386 Memory Management

- Both segmentation and paging
- Four views of the memory
 - Unsegmented and Unpaged
 - Virtual addresses are same as real addresses
 - Unsegmented paged
 - used by Berkeley UNIX
 - Segmented unpaged
 - Segmented and paged
 - used by Unix System 5

Summary

	TLB	First-level cache	Second-level cache	Virtual memory
Block size	4–8 bytes (1 PTE)	4–32 bytes	32–256 bytes	4096–16,384 bytes
Hit time	1 clock cycle	1–2 clock cycles	6–15 clock cycles	10–100 clock cycles
Miss penalty	10–30 clock cycles	8–66 clock cycles	30–200 clock cycles	700,000–6,000,000 clock cycles
Miss rate (local)	0.1–2%	0.5–20%	15–30%	0.00001–0.001%
Size	32–8192 bytes (8–1024 PTEs)	1–128 KB	256 KB–16 MB	16–8192 MB
Backing store	First-level cache	Second-level cache	Page-mode DRAM	Disks
Q1: block placement	Fully associative or set associative	Direct mapped	Direct mapped or set associative	Fully associative
Q2: block identification	Tag/block	Tag/block	Tag/block	Table
Q3: block replacement	Random	N.A. (direct mapped)	Random	= LRU
Q4: write strategy	Flush on a write to page table	Write through or write back	Write back	Write back