CMSC 411
Computer Systems Architecture
Lecture 20
Multiprocessors 2

Outline

- Review
- Coherence
- Write Consistency
- Snooping
- Building Blocks
- Snooping protocols and examples
- Coherence traffic and Performance on MP
- Directory-based protocols and examples
- Conclusion

Example Write Back Snoopy Protocol

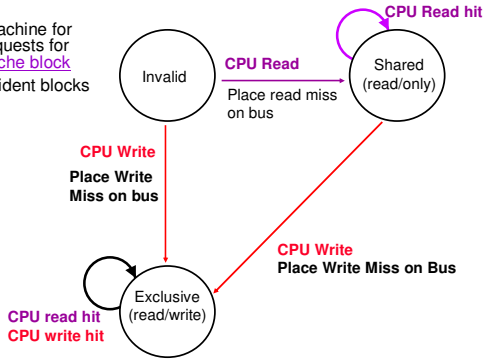
- Invalidation protocol, write-back cache
  - Snoops every address on bus
  - If it has a dirty copy of requested block, provides that block in response to the read request and aborts the memory access
- Each memory block is in one state:
  - Shared : Clean in all caches & up-to-date in memory
  - Exclusive : Dirty in exactly one cache
  - OR Not in any caches

Example Write Back Snoopy Protocol

- Each cache block is in one state (track these):
  - Shared : block can be read
  - Exclusive : cache has only copy, it is writeable & dirty
  - Invalid : block contains no data
    - » Also applies to uniprocessor cache
- Read misses: cause all caches to snoop bus
- Writes to clean blocks are treated as misses
  - write-allocate

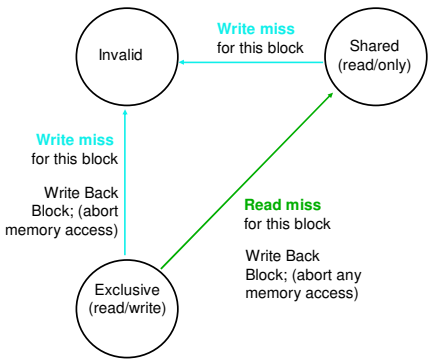
Write-Back State Machine – CPU Events

- State machine for *CPU* requests for each cache block
- Non-resident blocks invalid

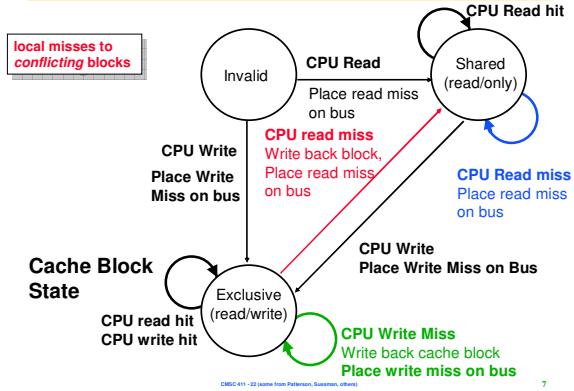


Write-Back State Machine- Bus events

State machine for *bus* requests for each cache block

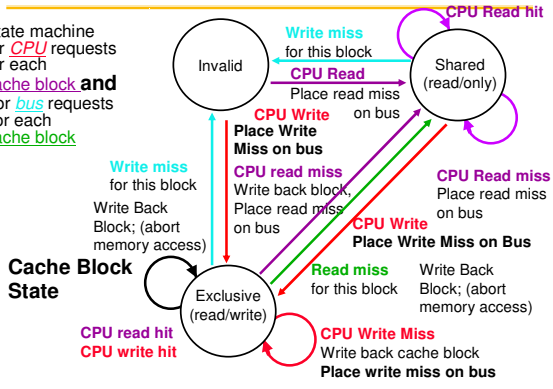


Block Replacement



Write-back State Machine-III

- State machine for *CPU* requests for each cache block **and** for *bus* requests for each cache block



Example

step	P1 State	P1 Addr	P1 Value	P2 State	P2 Addr	P2 Value	Bus Action	Bus Proc.	Bus Addr	Bus Value	Memory Addr	Memory Value
P1 Write 10 to A1											A1	0
P1: Read A1												
P2: Read A1												
P2: Write 20 to A1												
P2: Write 40 to A2												

Assumes A1 and A2 map to same cache block, initial cache state is invalid

Example

step	P1 State	P1 Addr	P1 Value	P2 State	P2 Addr	P2 Value	Bus Action	Bus Proc.	Bus Addr	Bus Value	Memory Addr	Memory Value
P1 Write 10 to A1	Excl.	A1	10				WrMs	P1	A1		A1	0
P1: Read A1												
P2: Read A1												
P2: Write 20 to A1												
P2: Write 40 to A2												

Assumes A1 and A2 map to same cache block

Example

step	P1 State	P1 Addr	P1 Value	P2 State	P2 Addr	P2 Value	Bus Action	Bus Proc.	Bus Addr	Bus Value	Memory Addr	Memory Value
P1 Write 10 to A1	Excl.	A1	10				WrMs	P1	A1		A1	0
P1: Read A1	Excl.	A1	10								A1	0
P2: Read A1												
P2: Write 20 to A1												
P2: Write 40 to A2												

Assumes A1 and A2 map to same cache block

Example

step	P1 State	P1 Addr	P1 Value	P2 State	P2 Addr	P2 Value	Bus Action	Bus Proc.	Bus Addr	Bus Value	Memory Addr	Memory Value
P1 Write 10 to A1	Excl.	A1	10				WrMs	P1	A1		A1	0
P1: Read A1	Excl.	A1	10								A1	0
P2: Read A1				Shar.	A1		RdMs	P2	A1		A1	0
	Shar.	A1	10				WrBk	P1	A1	10	A1	10
				Shar.	A1	10	RdDa	P2	A1	10	A1	10
P2: Write 20 to A1												
P2: Write 40 to A2												

Assumes A1 and A2 map to same cache block

Example

step	P1 State	P1 Addr	P1 Value	P2 State	P2 Addr	P2 Value	Bus Action	Bus Proc.	Bus Addr	Bus Value	Memory Addr	Memory Value
P1 Write 10 to A1	Excl.	A1	10				WrMs	P1	A1		A1	0
P1: Read A1	Excl.	A1	10								A1	0
P2: Read A1				Shar.	A1		RdMs	P2	A1		A1	0
	Shar.	A1	10				WrBk	P1	A1	10	A1	10
				Shar.	A1	10	RdDa	P2	A1	10	A1	10
P2: Write 20 to A1	Inv.			Excl.	A1	20	WrMs	P2	A1		A1	10
P2: Write 40 to A2												

Assumes A1 and A2 map to same cache block

Example

step	P1 State	P1 Addr	P1 Value	P2 State	P2 Addr	P2 Valu	Bus Actio	Bus Proc	Bus Addr	Bus Value	Memory Add	Memory Valu
P1 Write 10 to A1	Excl.	A1	10				WrMs	P1	A1		A1	0
P1: Read A1	Excl.	A1	10								A1	0
P2: Read A1				Shar.	A1		RdMs	P2	A1		A1	0
	Shar.	A1	10				WrBk	P1	A1	10	A1	10
				Shar.	A1	10	RdDa	P2	A1	10	A1	10
P2: Write 20 to A1	Inv.			Excl.	A1	20	WrMs	P2	A1		A1	10
P2: Write 40 to A2							WrBk	P2	A1	20	A1	20
				Excl.	A2	40	WrMs	P2	A2		A1	20

Assumes A1 and A2 map to same cache block, but A1 != A2

Write-back Invalidate Example

- Architecture
  - Simple bus-based symmetric multiprocessor
  - Each processor has a single private cache
  - Each cache is direct mapped
    - » addresses A1 & A2 are mapped to block B0
  - Coherence maintained with snooping
    - » Write-back

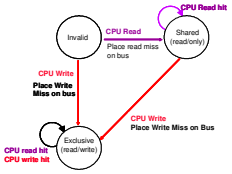
Write-Back Example: Time 0

Processor 0 Cache			
Block	State	Addr	Value
B0	Invalid	0	0

Processor 1 Cache			
Block	State	Addr	Value
B0	Invalid	0	0

Time	Proc	Action
1	P1	Write 10 to A1
2	P1	Read A1
3	P2	Read A1
4	P2	Write 20 to A1
5	P2	Write 40 to A2

Memory	
Addr	Value
A1	0
A2	0



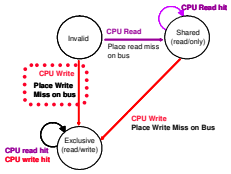
Write-Back Example: Time 1

Processor 0 Cache			
Block	State	Addr	Value
B0	Excl.	A1	10

Processor 1 Cache			
Block	State	Addr	Value
B0	Invalid	0	0

Time	Proc	Action
1	P1	Write 10 to A1
2	P1	Read A1
3	P2	Read A1
4	P2	Write 20 to A1
5	P2	Write 40 to A2

Memory	
Addr	Value
A1	0
A2	0



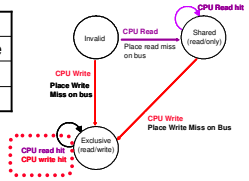
Write-Back Example: Time 2

Processor 0 Cache			
Block	State	Addr	Value
B0	Excl.	A1	10

Processor 1 Cache			
Block	State	Addr	Value
B0	Invalid	0	0

Time	Proc	Action
1	P1	Write 10 to A1
2	P1	Read A1
3	P2	Read A1
4	P2	Write 20 to A1
5	P2	Write 40 to A2

Memory	
Addr	Value
A1	0
A2	0



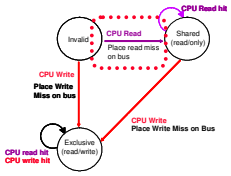
Write-Back Example: Time 3a

Processor 0 Cache			
Block	State	Addr	Value
B0	Excl.	A1	10

Processor 1 Cache			
Block	State	Addr	Value
B0	Share	A1	

Time	Proc	Action
1	P1	Write 10 to A1
2	P1	Read A1
3	P2	Read A1
4	P2	Write 20 to A1
5	P2	Write 40 to A2

Memory	
Addr	Value
A1	0
A2	0



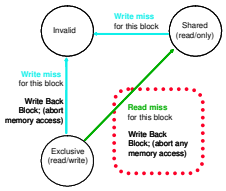
Write-Back Example: Time 3b

Processor 0 Cache			
Block	State	Addr	Value
B0	Share	A1	10

Processor 1 Cache			
Block	State	Addr	Value
B0	Share	A1	

Time	Proc	Action
1	P1	Write 10 to A1
2	P1	Read A1
3	P2	Read A1
4	P2	Write 20 to A1
5	P2	Write 40 to A2

Memory	
Addr	Value
A1	10
A2	0



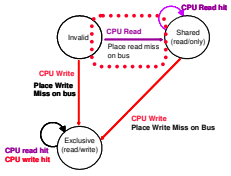
Write-Back Example: Time 3c

Processor 0 Cache			
Block	State	Addr	Value
B0	Share	A1	10

Processor 1 Cache			
Block	State	Addr	Value
B0	Share	A1	10

Time	Proc	Action
1	P1	Write 10 to A1
2	P1	Read A1
3	P2	Read A1
4	P2	Write 20 to A1
5	P2	Write 40 to A2

Memory	
Addr	Value
A1	10
A2	0



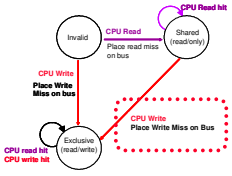
Write-Back Example: Time 4a

Processor 0 Cache			
Block	State	Addr	Value
B0	Share	A1	10

Processor 1 Cache			
Block	State	Addr	Value
B0	Excl.	A1	20

Time	Proc	Action
1	P1	Write 10 to A1
2	P1	Read A1
3	P2	Read A1
4	P2	Write 20 to A1
5	P2	Write 40 to A2

Memory	
Addr	Value
A1	10
A2	0



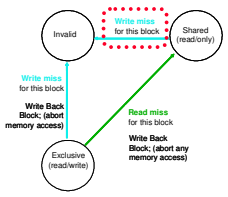
Write-Back Example: Time 4b

Processor 0 Cache			
Block	State	Addr	Value
B0	Invalid	A1	10

Processor 1 Cache			
Block	State	Addr	Value
B0	Excl.	A1	20

Time	Proc	Action
1	P1	Write 10 to A1
2	P1	Read A1
3	P2	Read A1
4	P2	Write 20 to A1
5	P2	Write 40 to A2

Memory	
Addr	Value
A1	10
A2	0



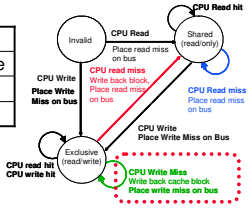
Write-Back Example: Time 5a

Processor 0 Cache			
Block	State	Addr	Value
B0	Invalid	A1	10

Processor 1 Cache			
Block	State	Addr	Value
B0	Excl.	A1	20

Time	Proc	Action
1	P1	Write 10 to A1
2	P1	Read A1
3	P2	Read A1
4	P2	Write 20 to A1
5	P2	Write 40 to A2

Memory	
Addr	Value
A1	20
A2	0



Write-Back Example: Time 5b

Processor 0 Cache			
Block	State	Addr	Value
B0	Invalid	A1	10

Processor 1 Cache			
Block	State	Addr	Value
B0	Excl.	A2	40

Time	Proc	Action
1	P1	Write 10 to A1
2	P1	Read A1
3	P2	Read A1
4	P2	Write 20 to A1
5	P2	Write 40 to A2

Memory	
Addr	Value
A1	20
A2	0