CMSC411 Spring 2011 Quiz 3

Name: ________________________________

You have 20 minutes to complete this quiz. You must show your work!

1. (9 pts) Cache organization

Suppose we have a byte addressable memory of size 4GB ($2^{32}$ bytes).

a. (4 pts) We are given a cache of size 1MB ($2^{20}$ bytes, not including tag bits) and a cache block size of 256 ($2^8$) bytes. Compute for a 8-way associative cache the length in number of bits for the tag, index and offset fields of a 32-bit memory address (show your calculations)

b. (2 pts) Considering the answer to part (a), circle the bits representing the index in the following 32-bit memory address (in binary):

$$1101110111000100111000111000111$$

c. (3 pts) Explain what the index of an address is used for, and why it does not need to be stored in the cache.
2. (4 pts) Cache performance

Suppose we have a cache / memory system with the following parameters:
- L1 cache with a 5% miss rate, cache hits require 1 clock cycle
- Clock rate of 1 GHz (1 clock cycle = 1 nanosecond)
- Memory system accesses require 20 nanoseconds

a. (2 pts) What is the average memory access time for the system?

b. (2 pts) We decide to add a second L2 cache that will be accessed only when accesses miss the L1 cache. If the L2 cache has a miss rate of 1%, what percentage of memory accesses will miss both caches and actually access memory?

3. (7 pts) Virtual memory organization

Suppose we have a virtual memory of size 4GB (2^{32} bytes).

a. (4 pts) Suppose pages are 8KB (2^{13} bytes) each, and the machine has 512MB (2^{29} bytes) of physical memory. Compute the number of page table entries needed if all the pages are being used. Compute the size of the page table if each page table entry also required 4 additional bits (valid, protection, dirty, use).

b. (3 pts) What is the function of a translation lookaside buffer (TLB), and why does it need to be performed quickly (e.g., 1-2 clock cycles)?