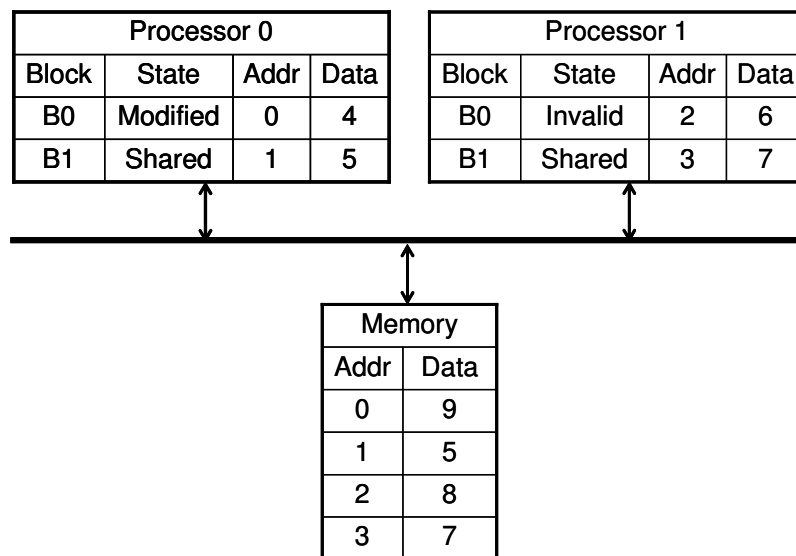


6. (30 pts) Multiprocessor cache coherency

Consider a simple bus-based symmetric multiprocessor, where each processor has a single private cache with coherence maintained with a snooping, write-back protocol. Each cache is direct mapped, with 2 blocks each holding 1 word (e.g., addrs 0 & 2 are mapped to block B0, addrs 1 & 3 are mapped to block B1).

For each question, assume the initial cache state is shown below. Show the resulting state of the caches and memory after each action. Show only the blocks that change. For instance, after [P0: read 3], the changes are [P0.B1: (Shared, 3, 7)], indicating Processor 0's block B1 now has the state = Shared, addr = 3, and data = 7. Also indicate the value returned by each read operation.



- a. Processor 1 reads 2
- b. Processor 1 writes 2 <- 10
- c. Processor 0 writes 1 <- 11
- d. Processor 1 writes 0 <- 12
- e. Processor 0 reads 2