



Lecture 10: Shared Memory Architectures

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Announcements

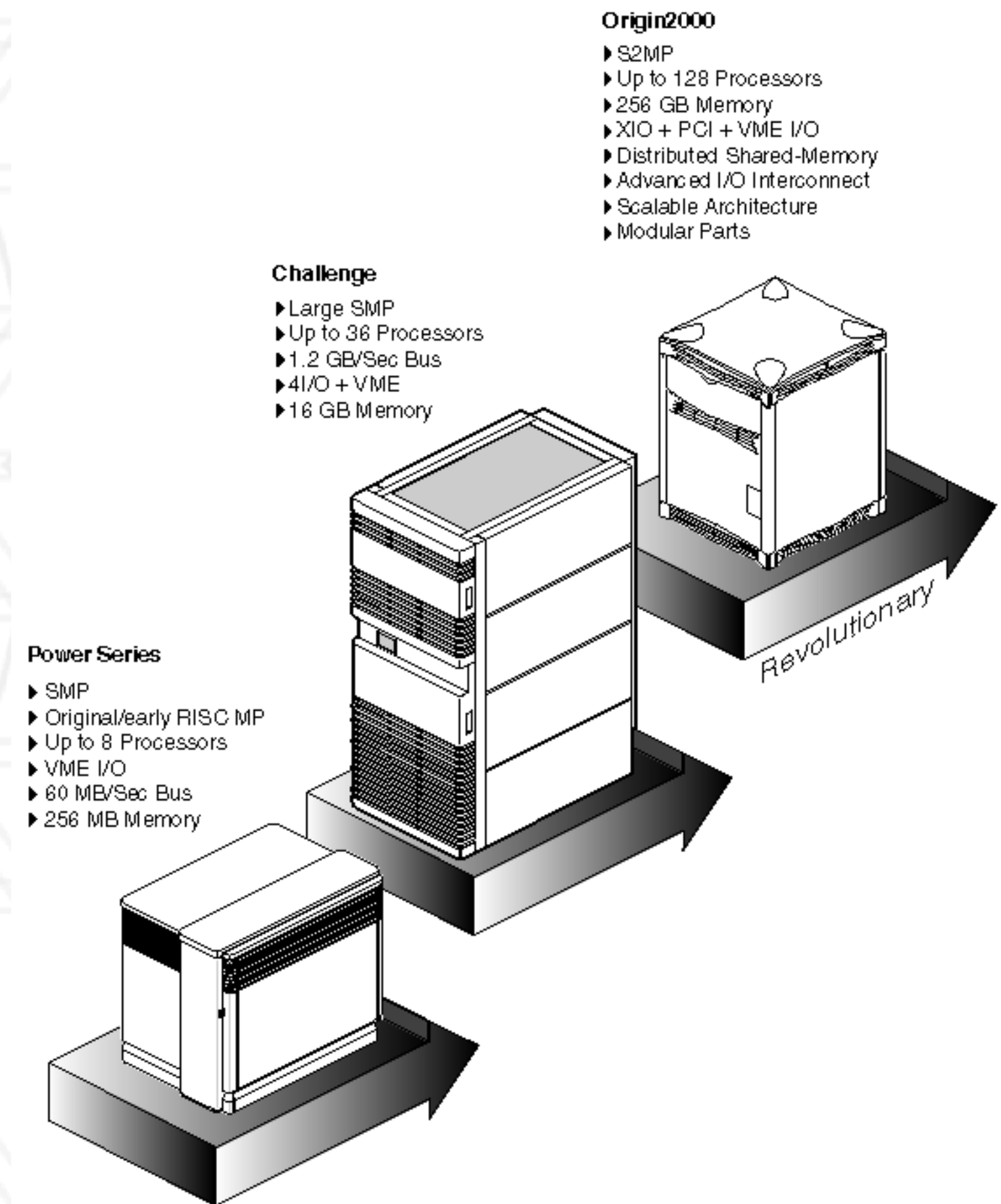
- Assignment 2 due on March 8
- Project description due on March 11

Summary of last lecture

- Single node architecture is fairly complex
 - Two product lines: fast processors, low frequency low power processors
- IBM Blue Gene/Q Compute Chip
- Accelerators: IBM Cell BE, AMD APUs, NVIDIA GPGPUs, Intel XE

Shared memory in hardware

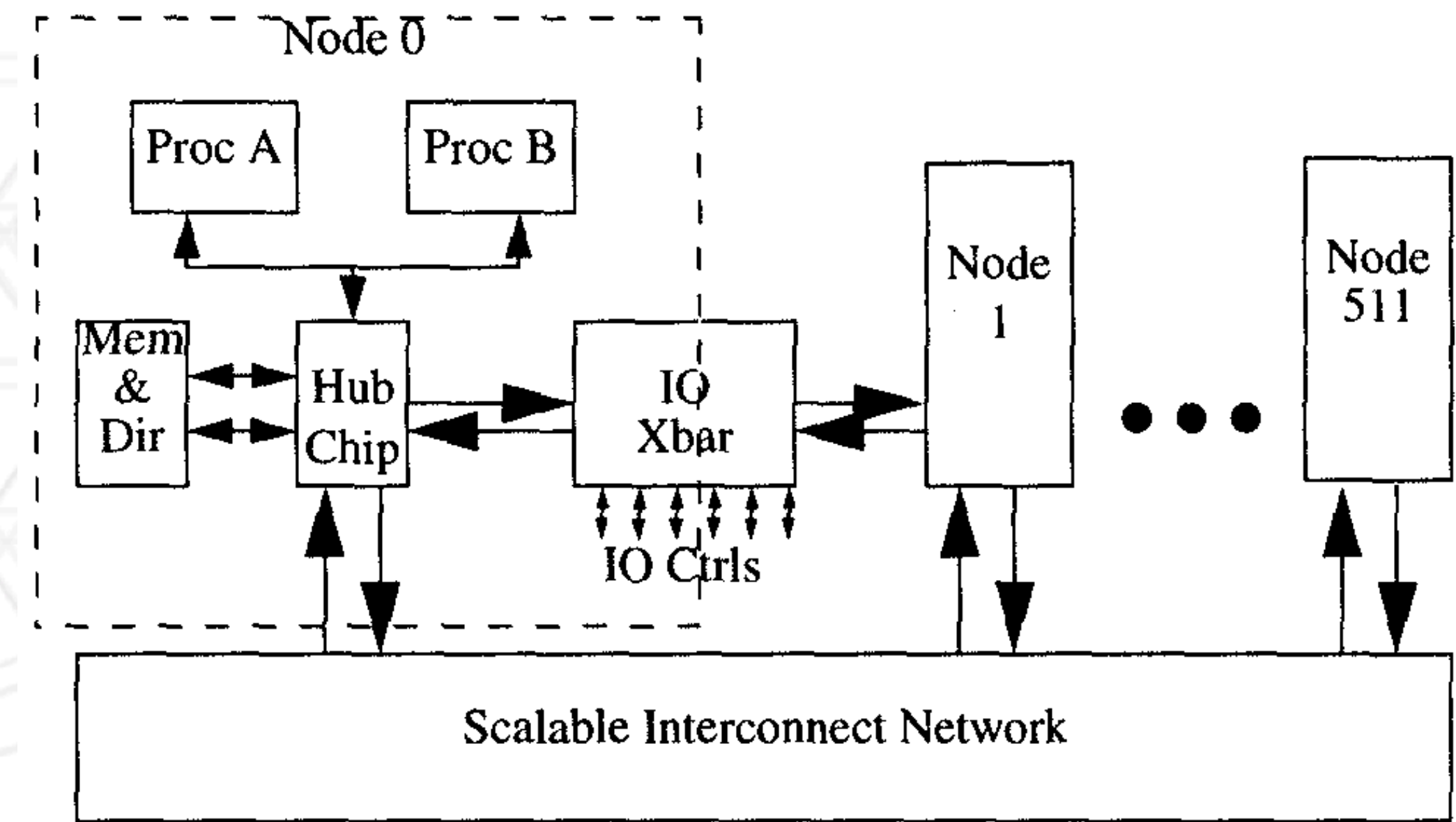
- Cache coherent globally addressable memory
- Older machines had bus-based symmetric multi-processing
- Origin was a different architecture: distributed shared memory with cache coherence



http://csweb.cs.wfu.edu/~torgerse/Kokua/SGI/007-3439-002/sgi_html/ch01.html

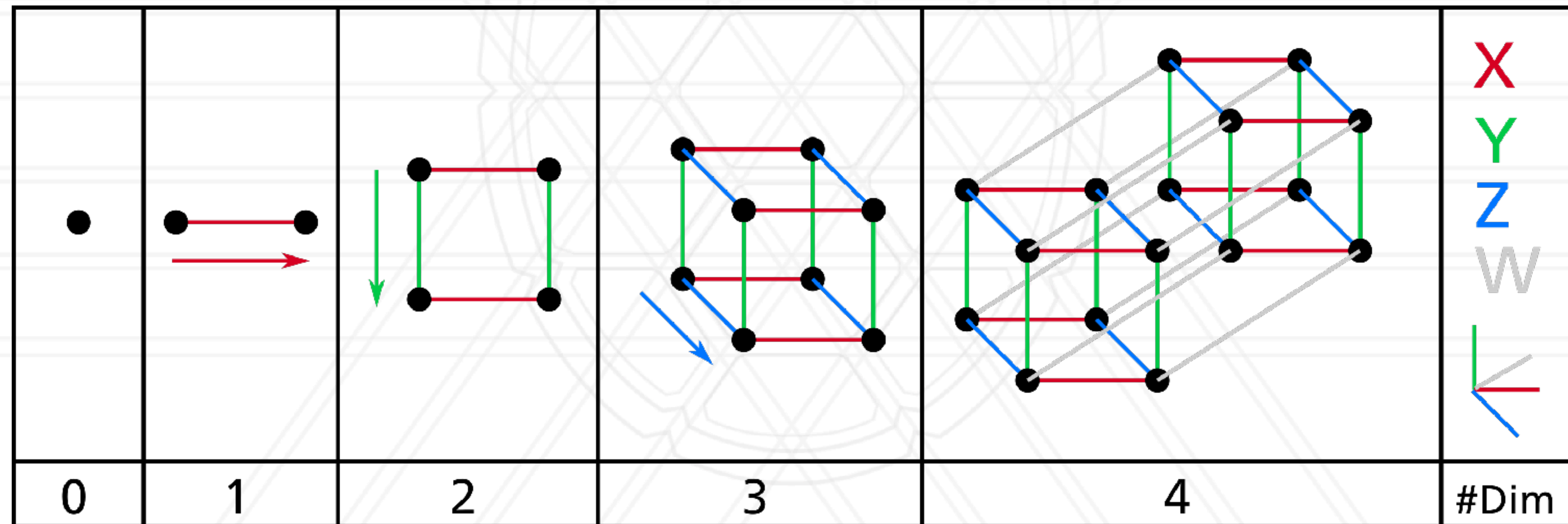
SGI Origin 2000

- Up to 512 nodes: 2 processors per node, 4 GB of memory
- Cache coherence maintained via a directory-based protocol
- Distributed directory that keeps track of each data block (page)
 - Implemented in hardware
 - Supports moving entire pages across nodes



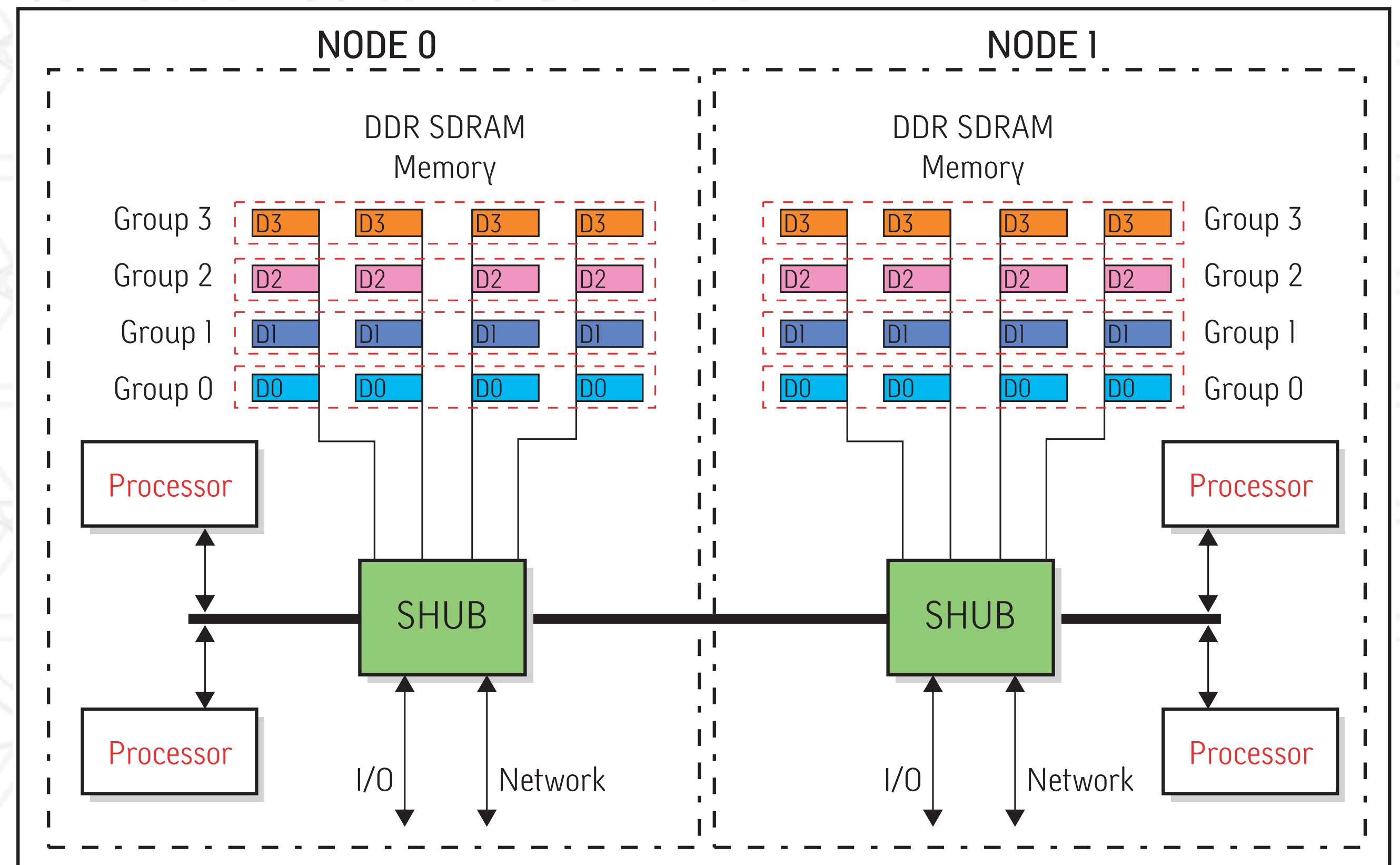
Hypercube network

- General topology: k -ary n -cube networks
- Hypercube: $k=2$

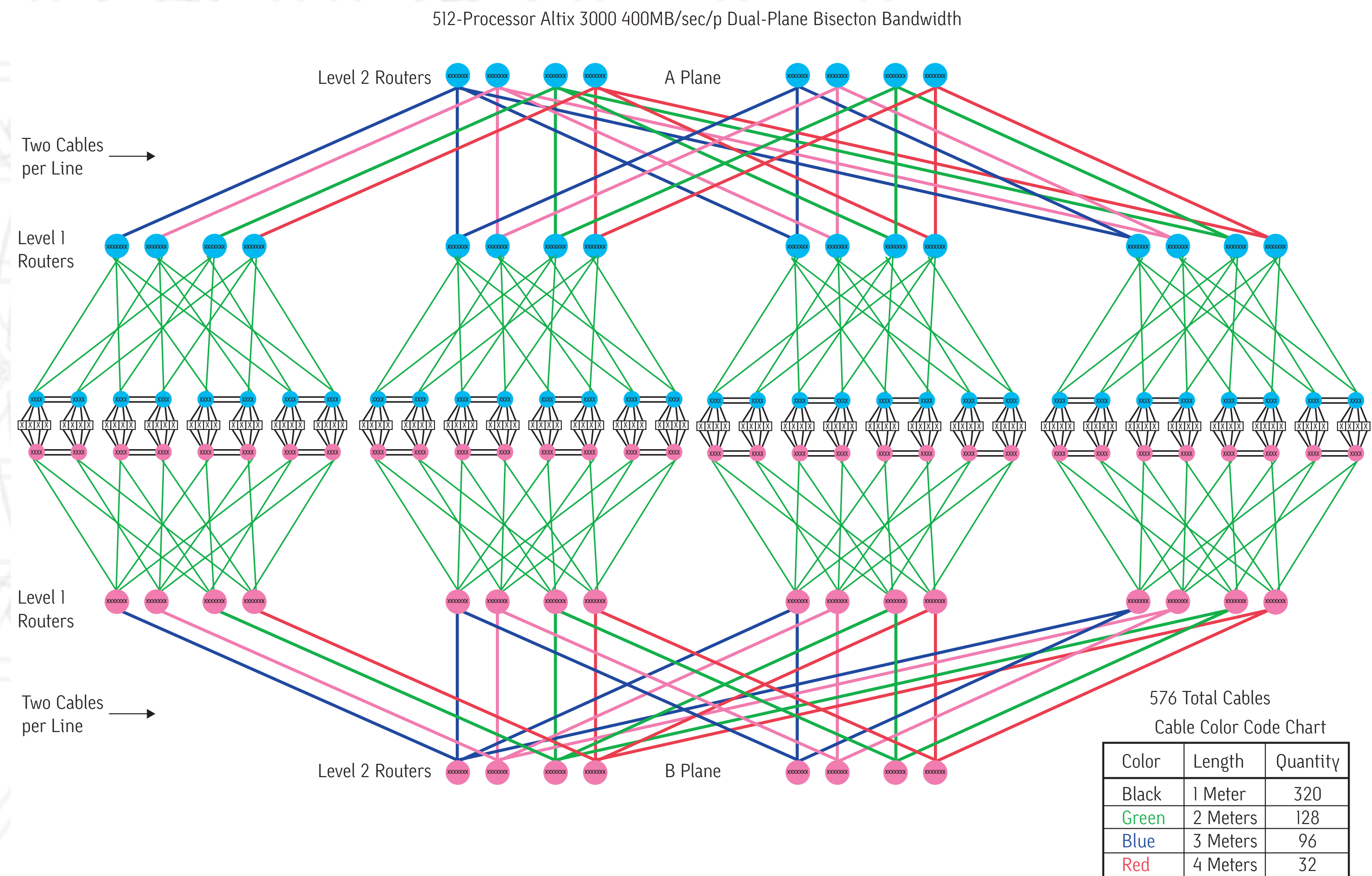


SGI Altix 3000

- Based on Intel Itanium 2 processors and Linux
- 4 processors and up to 32 GB of memory



Fat-tree network



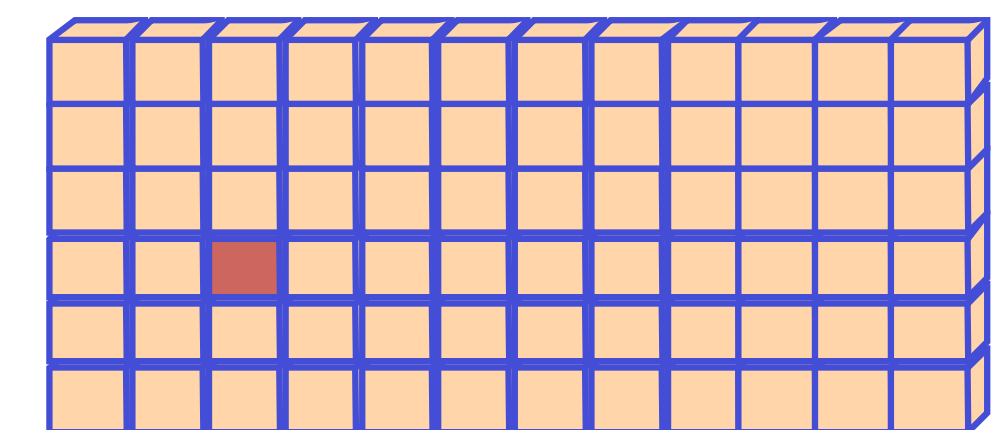
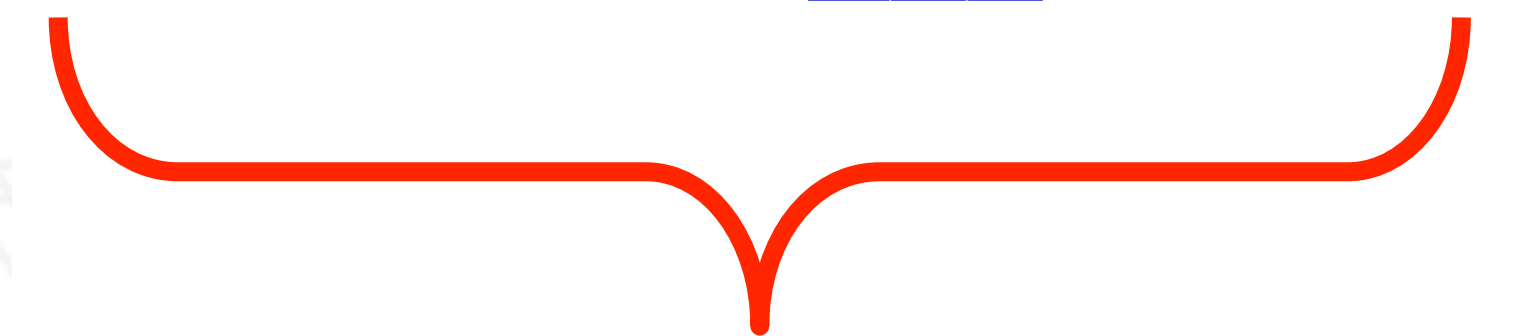
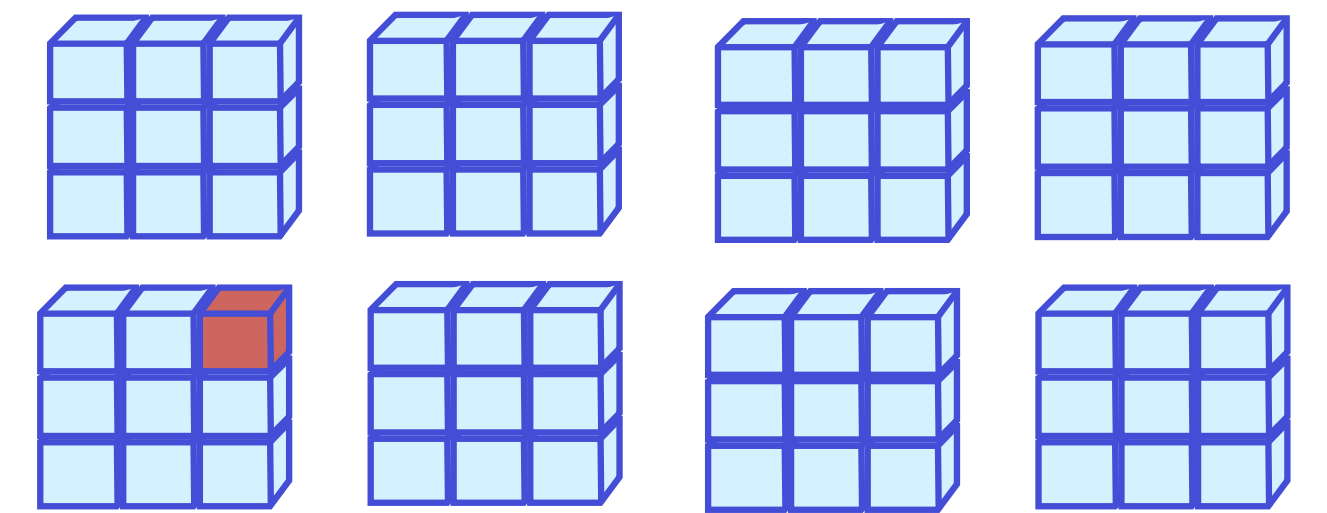
Partitioned global address space (PGAS)

- Another parallel programming model
- Globally addressable view of memory to the programmer
- Notable examples:
 - SUN's Fortress, IBM's XI0, Cray's Chapel
 - Unified Parallel C (UPC), Coarray Fortran (CAF), Global Arrays (GA)

Global Arrays

- Developed at PNNL
- CSE applications using it: NWChem, GAMESS-UK, Chimera
- Can only be used for arrays

Physically distributed data

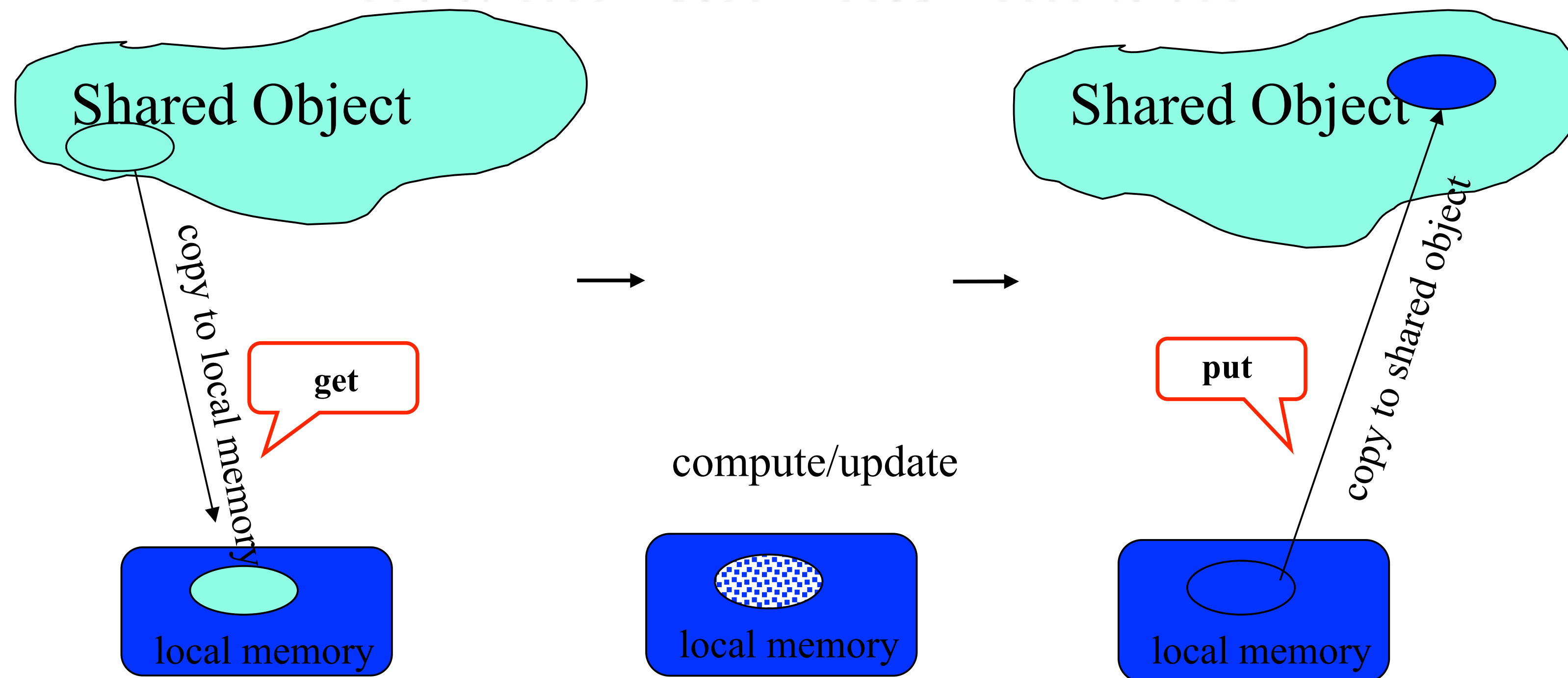


Global Address Space

https://www.osc.edu/sites/osc.edu/files/staff_files/dhudak/ga-osc11.pdf

Get-compute-put model

- Shared-memory view of distributed dense arrays



Questions?



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