

# ALRESCHA: A Lightweight Reconfigurable Sparse-Computation Accelerator

Bahar Asgari, Ramyad Hadidi,  
Tushar Krishna, Hyesoon Kim, and Sudhakar Yalamanchili



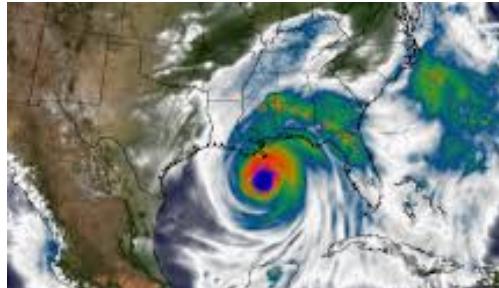




# Modeling impacts our lives and future!

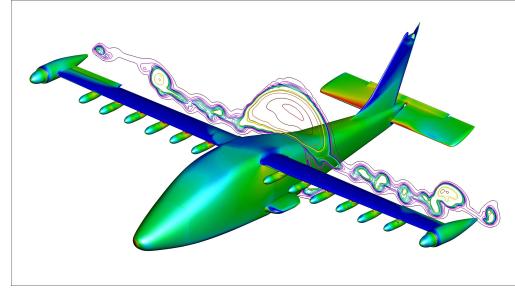
3

**Hurricanes**



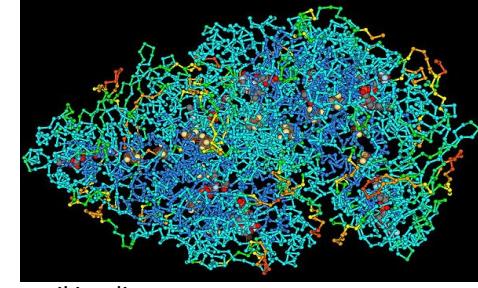
[nasa.gov](http://nasa.gov)

**Aerodynamic**



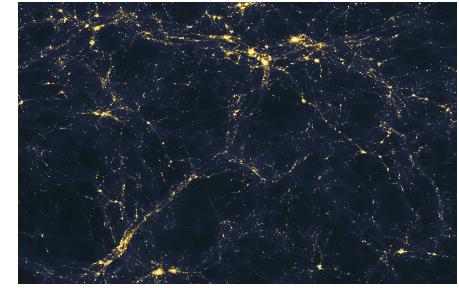
[nasa.gov](http://nasa.gov)

**Macromolecules**



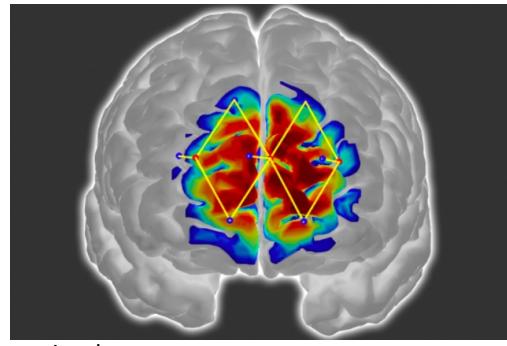
[wikipedia.org](http://wikipedia.org)

**Universe**



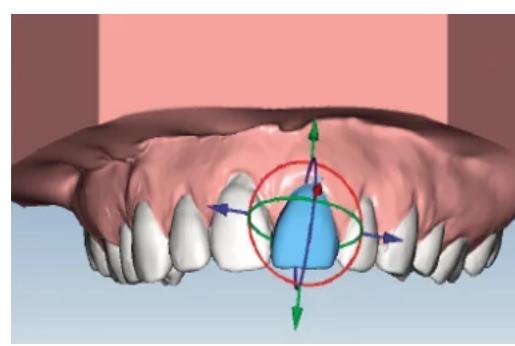
[ucl.ac.uk](http://ucl.ac.uk)

**Pain**



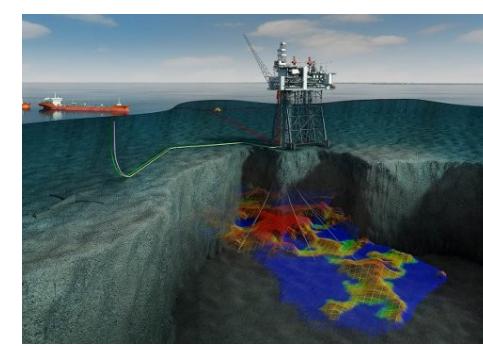
[mit.edu](http://mit.edu)

**Orthodontics**



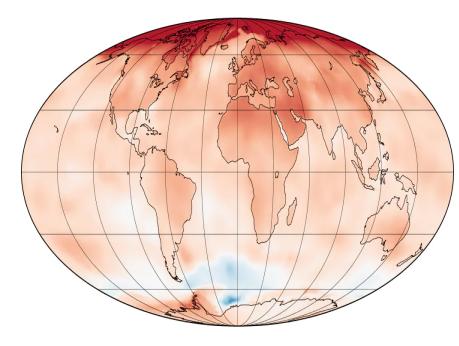
[planmeca.com](http://planmeca.com)

**Oil and Gas**



[enwa.com](http://enwa.com)

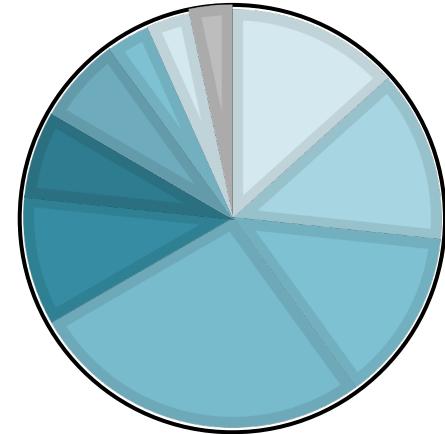
**Global Warming**



[washingtonpost.com](http://washingtonpost.com)



# Modeling is costly!



- Molecular Bioscience
- Chemistry
- Material Research
- Atmospheric Science
- Physics
- Astronomical Sciences
- Earth Sciences
- Chemical and Thermal Systems
- Advanced Scientific Computing
- Other

>96% of supercomputer workloads!<sup>1</sup>

\$3.5 million per year  
only for power and cooling  
one system<sup>2</sup>!

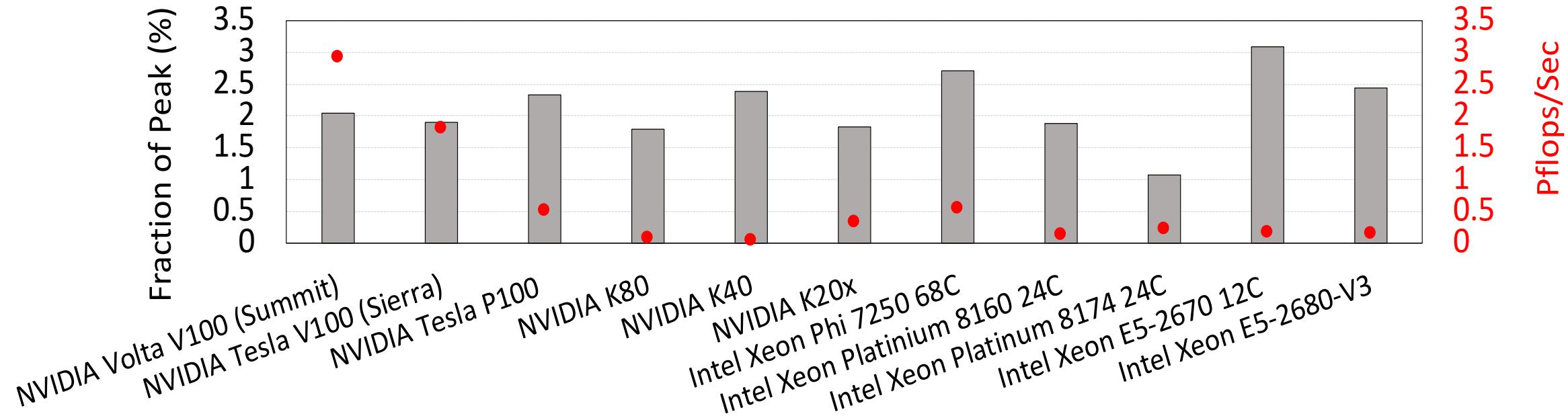


<sup>1</sup> Workloads of Kraken, housed in the Oak Ridge National Lab.

<sup>2</sup> Tianhe-1A



# Modeling is slow, even with optimizations!



They utilize < 3% of peak performance

Data obtained from HPCG ranking.



We propose Alrescha<sup>1</sup>  
a **fast** and **low-cost** solution  
for executing scientific problems

<sup>1</sup>Alrescha (/æl'ri:ʃə/) is a binary star system in the equatorial constellation of Pisces



# Outline

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- ▶ Using PDEs for modeling and key challenges
- ▶ Alrescha
  - ▶ Main contributions
  - ▶ Storage format
  - ▶ Reconfigurable microarchitecture
  - ▶ Broad applications
- ▶ Results
- ▶ Conclusions



# Outline

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- ▶ **Using PDEs for modeling and key challenges**
- ▶ Alrescha
  - ▶ Main contributions
  - ▶ Storage format
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  - ▶ Broad applications
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# Partial differential equations (PDEs)

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- ▶ PDEs are used for modeling.
- ▶ PDEs are transformed to  $Ax = b$ .

## ▶ Solving PDEs

Focus of this paper →

Direct methods: Exact but too slow 🤔

- Cholesky method
- Are not used for large sparse problems

Iterative methods: Fast and converges 😊

- Conjugated Gradient (CG)
- Fast execution → more iterations → exact results



# PDE Characteristics and Challenges

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- ▶ PDEs are **sparse**
- ▶ Iterative solvers include **data-dependency**
  
- ▶ Limited parallelism:
  - ▶ **Dependencies** limit using high memory bandwidth
  
- ▶ We cannot simply add more bandwidth to gain performance



# Dependencies in solving PDEs

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Symmetric Gauss Seidel (SymGS) is the main kernel

Simplified mathematical expression is  $x_i = \sum_{j=0}^{\text{columns}} A_{ij}^T \times x_j$

Which includes a nested loop:

- ▶ Iterations of **outer** loop are **data-dependent** This creates bottleneck
- ▶ Iterations of **inner** loop can run in **parallel**

```
for i = 0 to rows
    for j = 0 to columns
        sum += A[i][j] * x[j]
    x[i] = update(sum)
```

The equation and pseudo are the extremely simplified version of SymGS



# Why data-dependent?

12

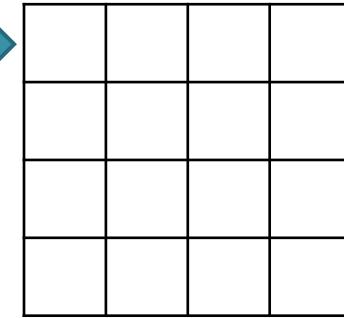
At each iteration of the outer loop, we

- ▶ Read entire  $x$
- ▶ Update one element of  $x$

```
for i = 0 to rows
    for j = 0 to columns
        sum += A[i][j] * x[j]
        x[i] = update(sum)
```

Matrix  $A$ :

$i = 0$  ➔



Vector  $x$ :



read

The pseudo is the extremely simplified version of SymGS



# Why data-dependent?

13

At each iteration of the outer loop, we

- ▶ Read entire  $x$
- ▶ Update one element of  $x$

```
for i = 0 to rows
    for j = 0 to columns
        sum += A[i][j] * x[j]
    x[i] = update(sum)
```

Matrix  $A$ :

$i = 0 \rightarrow$


Vector  $x$ :

update			

The pseudo is the extremely simplified version of SymGS



# Why data-dependent?

14

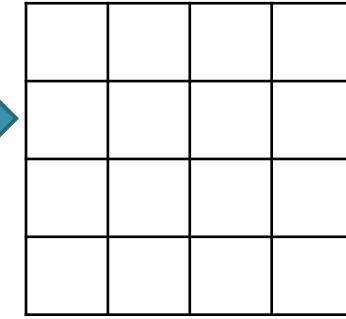
At each iteration of the outer loop, we

- ▶ Read entire  $x$
- ▶ Update one element of  $x$

```
for i = 0 to rows
    for j = 0 to columns
        sum += A[i][j] * x[j]
        x[i] = update(sum)
```

Matrix  $A$ :

$i = 1$



Vector  $x$ :



The pseudo is the extremely simplified version of SymGS



# Why data-dependent?

15

At each iteration of the outer loop, we

- ▶ Read entire  $x$
- ▶ Update one element of  $x$

```
for i = 0 to rows
    for j = 0 to columns
        sum += A[i][j] * x[j]
    x[i] = update(sum)
```

Matrix  $A$ :

$i = 1$  


Vector  $x$ :



The pseudo is the extremely simplified version of SymGS



# Why data-dependent?

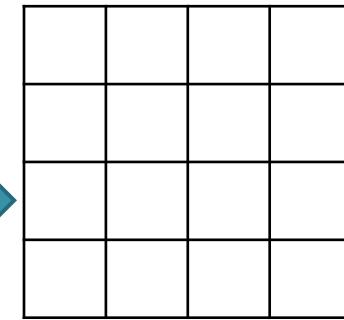
At each iteration of the outer loop, we

- ▶ Read entire  $x$
- ▶ Update one element of  $x$

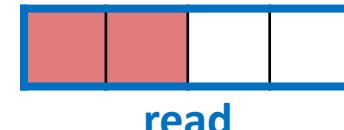
```
for i = 0 to rows
    for j = 0 to columns
        sum += A[i][j] * x[j]
        x[i] = update(sum)
```

Matrix  $A$ :

$i = 2$



Vector  $x$ :





# Why data-dependent?

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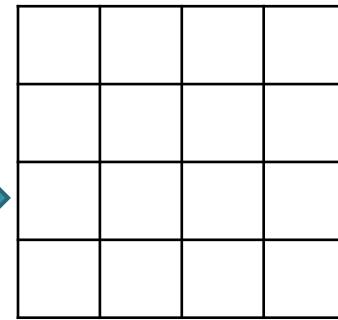
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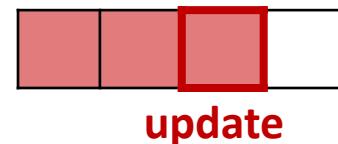
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```

Matrix  $A$ :

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Vector  $x$ :



The pseudo is the extremely simplified version of SymGS



# Why data-dependent?

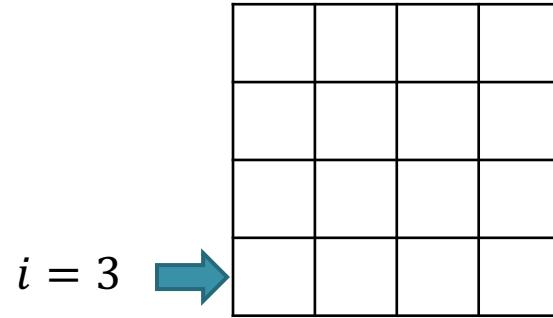
18

At each iteration of the outer loop, we

- ▶ Read entire  $x$
- ▶ Update one element of  $x$

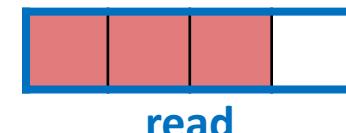
```
for i = 0 to rows  
    for j = 0 to columns  
        sum += A[i][j] * x[j]  
  
        x[i] = update(sum)
```

Matrix  $A$ :



$i = 3$  →

Vector  $x$ :



read

The pseudo is the extremely simplified version of SymGS



# Why data-dependent?

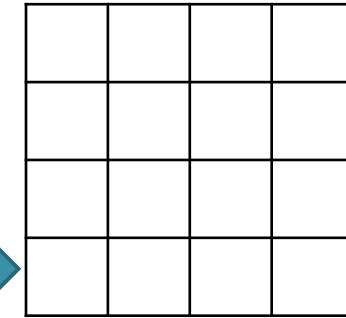
At each iteration of the outer loop, we

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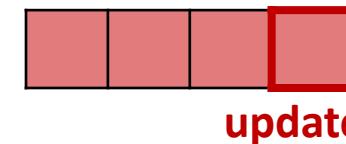
```
for i = 0 to rows
    for j = 0 to columns
        sum += A[i][j] * x[j]
    x[i] = update(sum)
```

Matrix  $A$ :

$i = 3$  



Vector  $x$ :





# Cannot utilize parallelism of GPU

20

## Timeline of GPU:

```
for i = 0 to rows  
    for j = 0 to columns  
        x[i] = ...
```



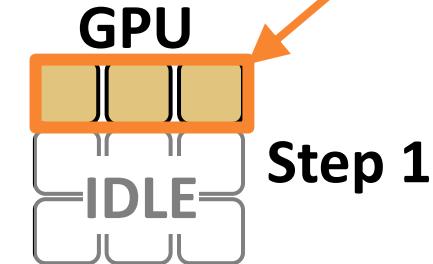
**Iterations of outer loop**

i = 4

for j = 0 to columns

x[4]=...

Inner loop runs in parallel





# Cannot utilize parallelism of GPU

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## Timeline of GPU:

```
for i = 0 to rows  
    for j = 0 to columns  
        x[i] = ...
```



**Iterations of outer loop**

i = 4

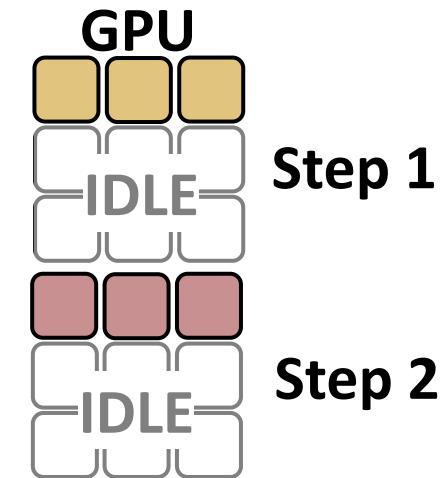
for j = 0 to columns

x[4]=...

i = 5

for j = 0 to columns

x[5]=...





# Cannot utilize parallelism of GPU

22

## Timeline of GPU:

```
for i = 0 to rows  
    for j = 0 to columns  
        x[i] = ...
```



**Iterations of outer loop**

i = 4

for j = 0 to columns

x[4]=...

i = 5

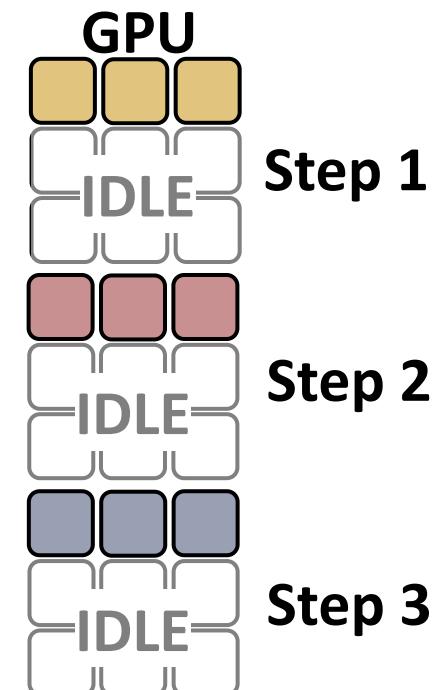
for j = 0 to columns

x[5]=...

i = 6

for j = 0 to columns

x[6]=...





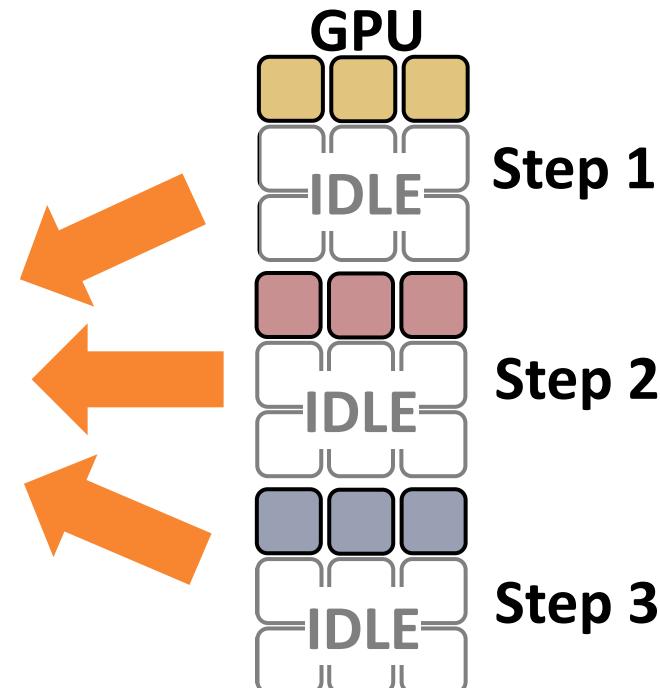
# Key challenge

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## Timeline of GPU:

```
for i = 0 to rows  
    for j = 0 to columns  
        x[i] = ...
```

Iterations of the outer loop  
are not parallel





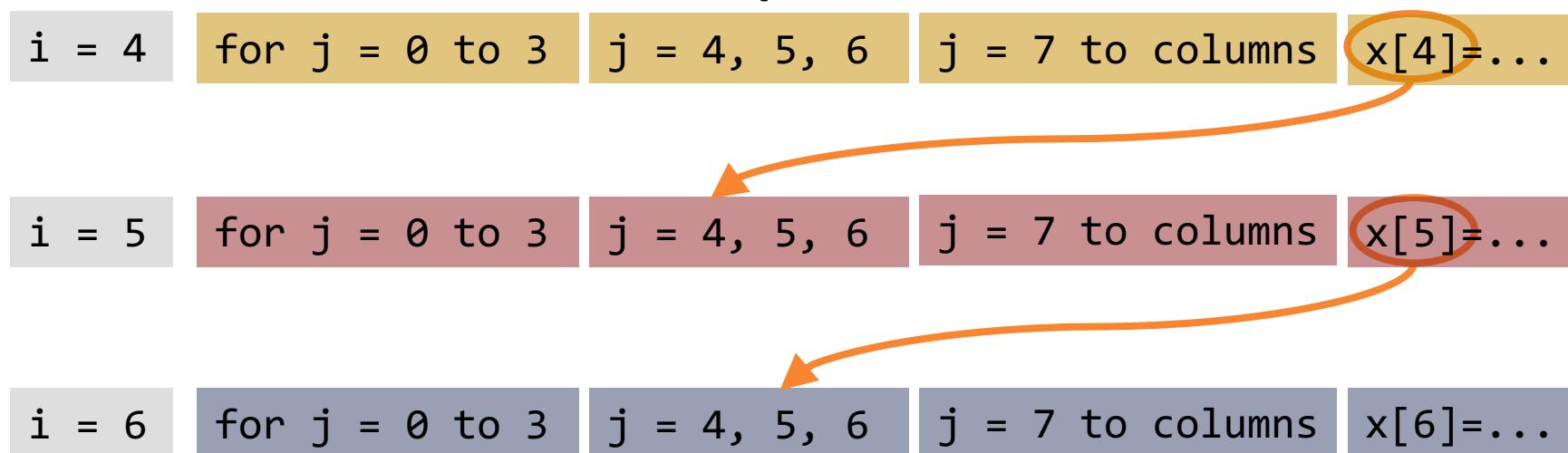
# Optimization cannot help

24

## Timeline of GPU with unrolling and blocking:

```
for i = 0 to rows
    for j = 0 to columns
        x[i] = ...
```

↓ **Unroll the outer loop &  
Break down the inner loop**



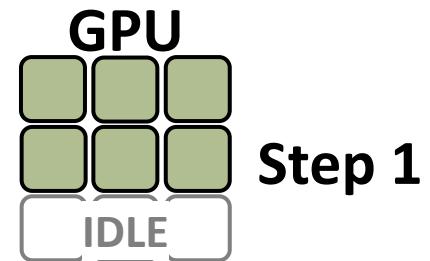
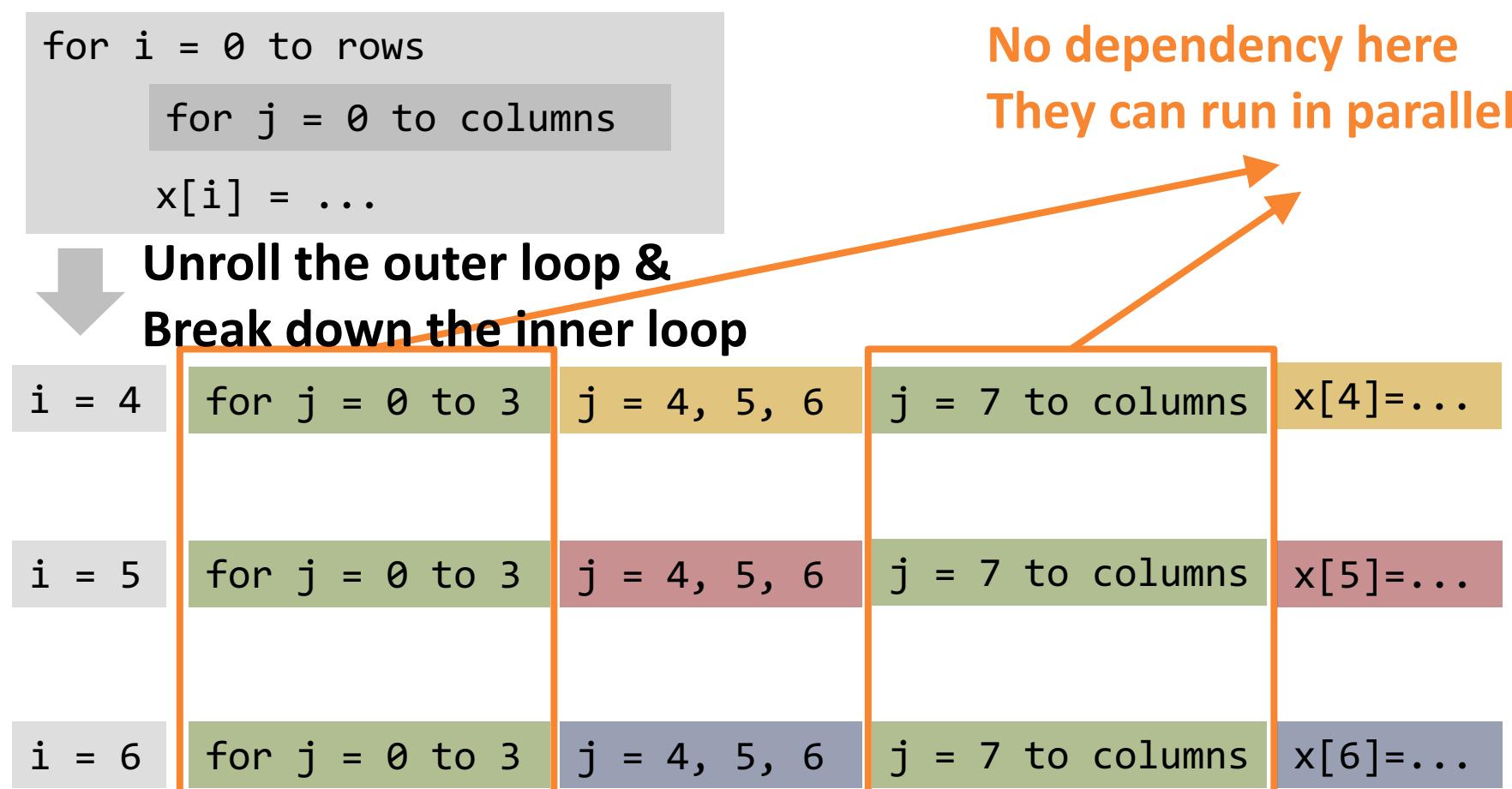
Optimizations similar to graph coloring



# Optimization cannot help

25

## Timeline of GPU with unrolling and blocking:



Optimizations similar to graph coloring



# Optimization cannot help

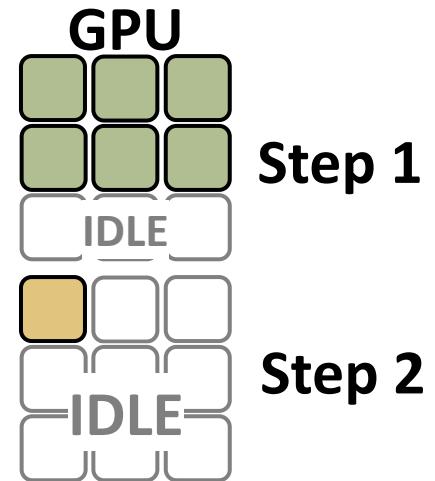
26

## Timeline of GPU with unrolling and blocking:

```
for i = 0 to rows
    for j = 0 to columns
        x[i] = ...
```

↓ **Unroll the outer loop &  
Break down the inner loop**

```
i = 4    for j = 0 to 3  j = 4, 5, 6  j = 7 to columns  x[4]=...
```



```
i = 5    for j = 0 to 3  j = 4, 5, 6  j = 7 to columns  x[5]=...
```

```
i = 6    for j = 0 to 3  j = 4, 5, 6  j = 7 to columns  x[6]=...
```

Optimizations similar to graph coloring



# Optimization cannot help

27

## Timeline of GPU with unrolling and blocking:

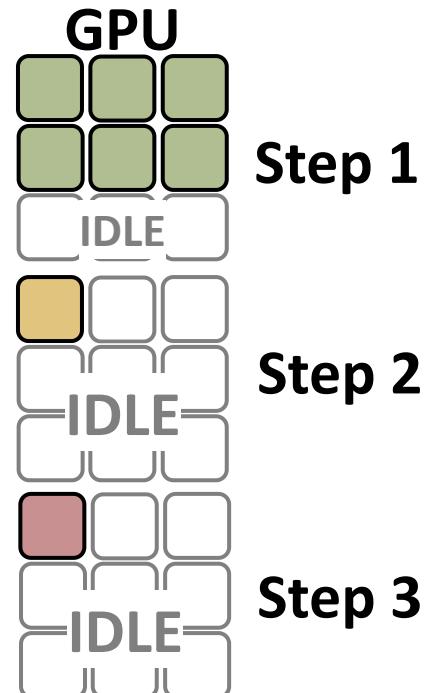
```
for i = 0 to rows
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```

↓ **Unroll the outer loop &  
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i = 4    for j = 0 to 3    j = 4, 5, 6    j = 7 to columns    x[4]=...
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```
i = 6    for j = 0 to 3    j = 4, 5, 6    j = 7 to columns    x[6]=...
```



Optimizations similar to graph coloring



# Optimization cannot help

28

## Timeline of GPU with unrolling and blocking:

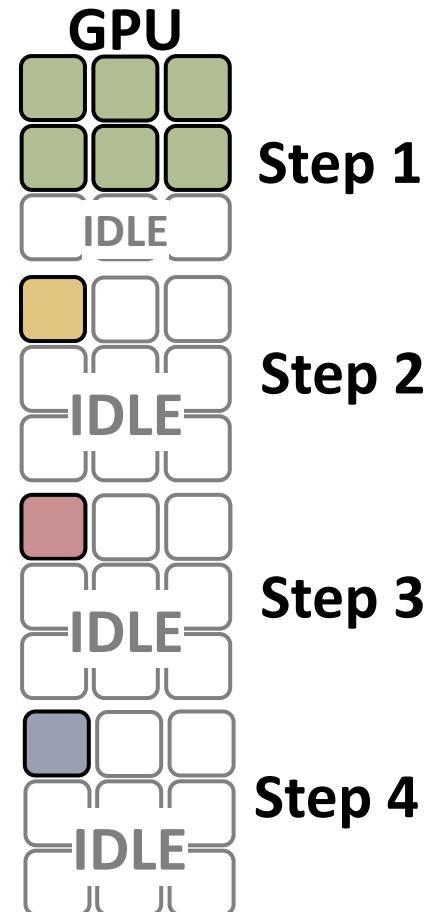
```
for i = 0 to rows
    for j = 0 to columns
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```

↓ **Unroll the outer loop &  
Break down the inner loop**

```
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```
i = 6    for j = 0 to 3    j = 4, 5, 6    j = 7 to columns    x[6]=...
```



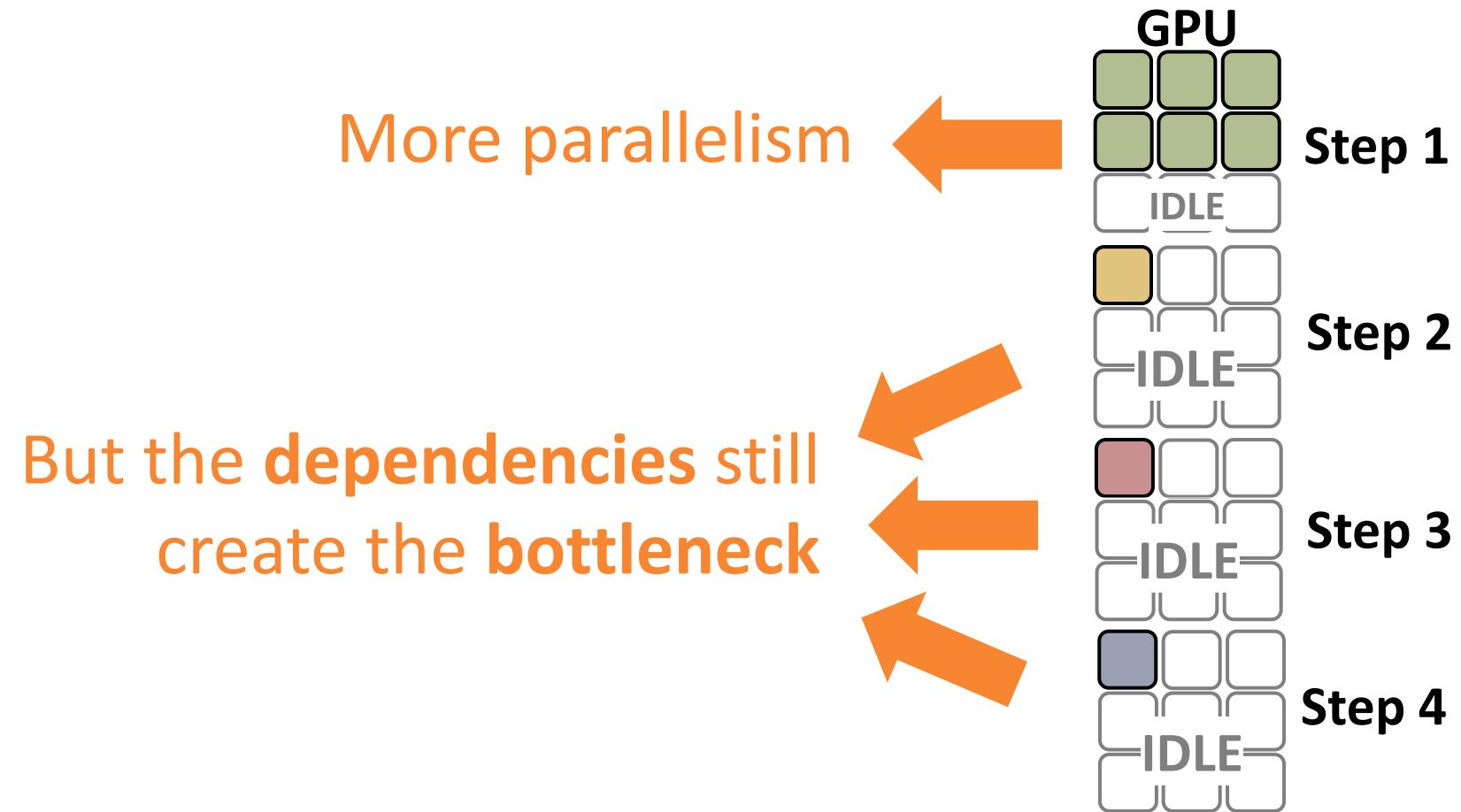
Optimizations similar to graph coloring



# Key challenge

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Timeline of GPU with unrolling and blocking:





# Key insight

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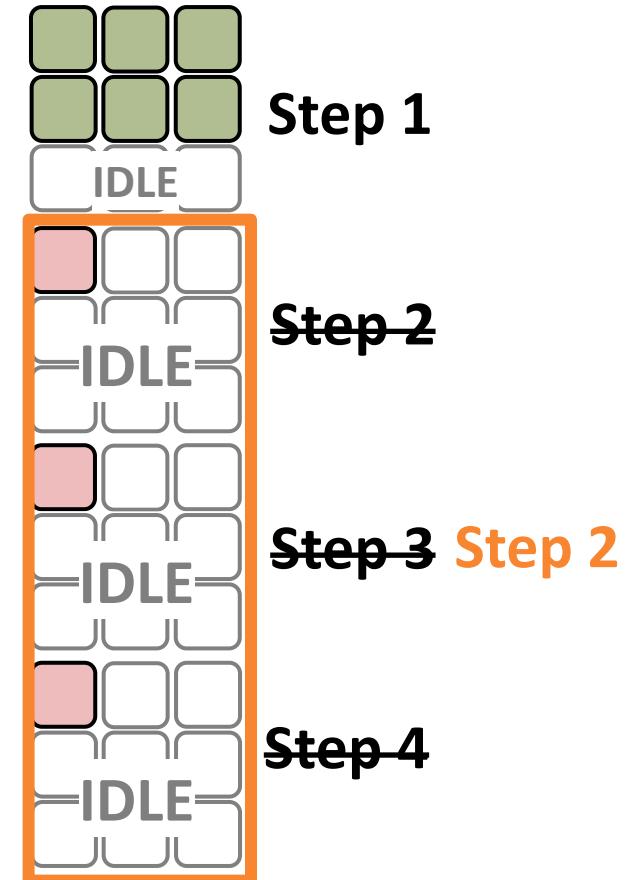
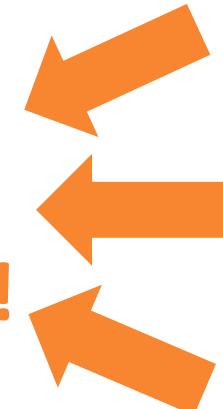
We accelerate the dependent operations

We use a partially reconfigurable hardware  
to execute both parallel and dependent part

We cannot resolve dependencies

but,

We can execute them in one step!





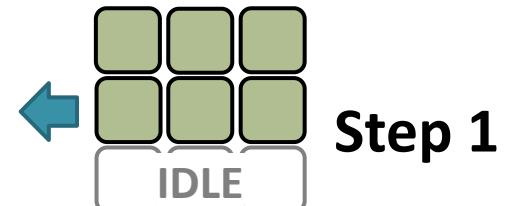
# Alrescha

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Divides a large SymGS into:

- ▶ Parallel **GEMV<sup>1</sup>**
- ▶ Small data-dependent **SymGS<sup>2</sup>**

$$\text{GEMV} \quad x'_i = \sum_{j \neq 4,5,6} A_{ij}^T \times x_j$$



Reorders the operations:

- ▶ First, GEMV
- ▶ Then, SymGS

$$\begin{aligned} \overline{x_4} &= x'_4 + A_{44}^T \times x_4 + A_{45}^T \times x_5 + A_{46}^T \times x_6 \\ \overline{x_5} &= x'_5 + A_{54}^T \times \overline{x_4} + A_{55}^T \times x_5 + A_{56}^T \times x_6 \\ \overline{x_6} &= x'_6 + A_{64}^T \times \overline{x_4} + A_{65}^T \times \overline{x_5} + A_{66}^T \times x_6 \end{aligned}$$

<sup>1</sup>GEMV: General matrix vector multiplication

<sup>2</sup>SymGS: Symmetric Gauss Seidel



# Outline

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- ▶ Using PDEs for modeling and key challenges
- ▶ Alrescha
  - ▶ Main contributions
  - ▶ Storage format
  - ▶ Reconfigurable microarchitecture
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- ▶ Conclusions



# Contributions of Alrescha

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1. To take advantage of reordering
  - ▶ Fast execution of data-dependent SymGS

$$x'_i = \sum_{j \neq 4,5,6} A_{ij}^T \times x_j$$

The diagram illustrates the computation of three variables  $\bar{x}_4$ ,  $\bar{x}_5$ , and  $\bar{x}_6$  based on their previous values and matrix-vector products. The variables are represented by orange circles, and the dependencies are shown by orange arrows. The background is shaded pink.

$$\bar{x}_4 = x'_4 + A_{44}^T \times x_4 + A_{45}^T \times x_5 + A_{46}^T \times x_6$$
$$\bar{x}_5 = x'_5 + A_{54}^T \times \bar{x}_4 + A_{55}^T \times x_5 + A_{56}^T \times x_6$$
$$\bar{x}_6 = x'_6 + A_{64}^T \times \bar{x}_4 + A_{65}^T \times \bar{x}_5 + A_{66}^T \times x_6$$

Dependencies still exist  
Alrescha implements them fast!



# Contributions of Alrescha

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## 1. To take advantage of reordering

- ▶ Fast execution of data-dependent SymGS
- ▶ Fast switching between GEMV to SymGS

This must be fast!  
Alrescha uses a LIFO<sup>1</sup>

$$x'_i = \sum_{j=4,5,6} A_{ij}^T \times x_j$$
$$\bar{x}_4 = x'_4 + A_{44}^T \times x_4 + A_{45}^T \times x_5 + A_{46}^T \times x_6$$
$$\bar{x}_5 = x'_5 + A_{54}^T \times \bar{x}_4 + A_{55}^T \times x_5 + A_{56}^T \times x_6$$
$$\bar{x}_6 = x'_6 + A_{64}^T \times \bar{x}_4 + A_{65}^T \times \bar{x}_5 + A_{66}^T \times x_6$$

<sup>1</sup>Last in first out (LIFO) buffer



# Contributions of Alrescha

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## 1. Reordering the operations

- ▶ Fast execution of data-dependent SymGS
- ▶ Fast switching between GEMV to SymGS

## 2. Lightweight reconfigurable architecture

- ▶ A fixed reduction engine
- ▶ A small reconfigurable hardware

They differ slightly  
Both need reduction!



$$x'_i = \sum_{j \neq 4,5,6} A_{ij}^T \times x_j$$

$$\overline{x_4} = x'_4 + A_{44}^T \times x_4 + A_{45}^T \times x_5 + A_{46}^T \times x_6$$

$$\overline{x_5} = x'_5 + A_{54}^T \times \overline{x_4} + A_{55}^T \times x_5 + A_{56}^T \times x_6$$

$$\overline{x_6} = x'_6 + A_{64}^T \times \overline{x_4} + A_{65}^T \times \overline{x_5} + A_{66}^T \times x_6$$



# Contributions of Alrescha

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## 1. Reordering the operations

- ▶ Fast execution of data-dependent SymGS
- ▶ Fast switching between GEMV to SymGS

## 2. Lightweight reconfigurable architecture

- ▶ A fixed reduction engine
- ▶ A small reconfigurable hardware

## 3. A new storage format

- ▶ To sustain the desired orders

$$x'_i = \sum_{j \neq 4,5,6} A_{ij}^T \times x_j$$

$$\overline{x_4} = x'_4 + A_{44}^T \times x_4 + A_{45}^T \times x_5 + A_{46}^T \times x_6$$

$$\overline{x_5} = x'_5 + A_{54}^T \times \overline{x_4} + A_{55}^T \times x_5 + A_{56}^T \times x_6$$

$$\overline{x_6} = x'_6 + A_{64}^T \times \overline{x_4} + A_{65}^T \times \overline{x_5} + A_{66}^T \times x_6$$



# Contributions of Alrescha

37

## 1. Reordering the operations

- ▶ Fast execution of data-dependent SymGS
- ▶ Fast switching between GEMV to SymGS

## 2. Lightweight reconfigurable architecture

- ▶ A fixed reduction engine
- ▶ A small reconfigurable hardware

## 3. A new storage format

- ▶ To sustain the desired orders

## 4. Broad applications

- ▶ Because we have a reduction engine!

$$x'_i = \sum_{j \neq 4,5,6} A_{ij}^T \times x_j$$

$$\overline{x_4} = x'_4 + A_{44}^T \times x_4 + A_{45}^T \times x_5 + A_{46}^T \times x_6$$

$$\overline{x_5} = x'_5 + A_{54}^T \times \overline{x_4} + A_{55}^T \times x_5 + A_{56}^T \times x_6$$

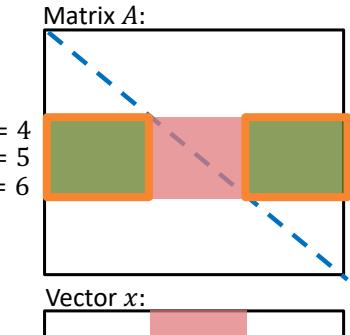
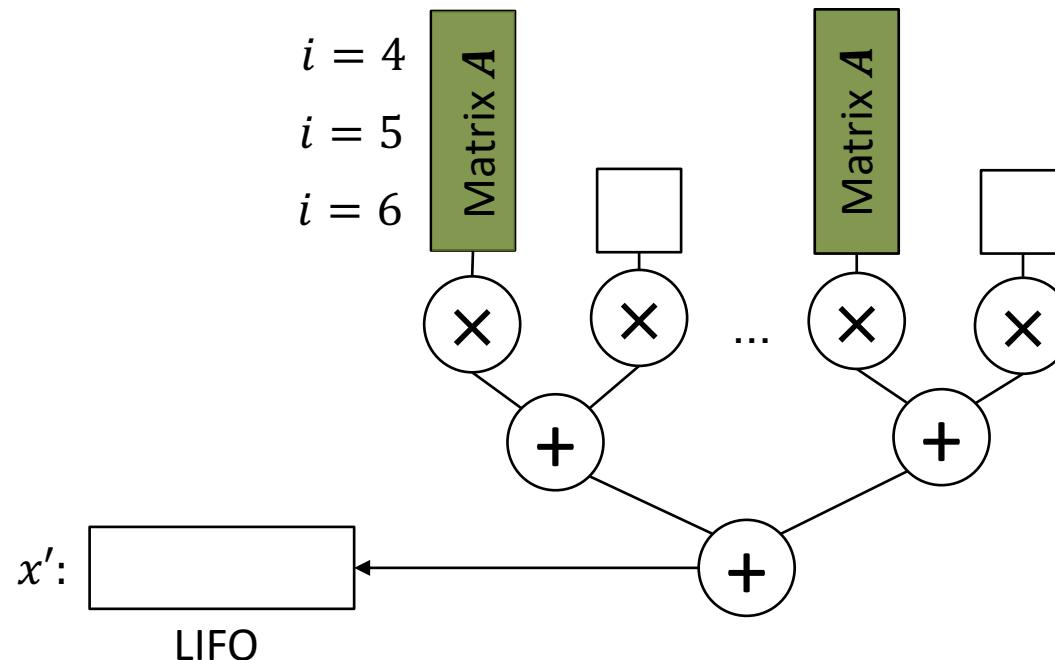
$$\overline{x_6} = x'_6 + A_{64}^T \times \overline{x_4} + A_{65}^T \times \overline{x_5} + A_{66}^T \times x_6$$



# Reordering the operations

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- ▶ First, Alrescha
  - ▶ Executes the GEMV
  - ▶ Produces intermediate results (partial sum,  $x'$ )
  - ▶ Pushes  $x'$  into a LIFO to reuse them fast, later



$$x'_i = \sum_{j \neq 4,5,6} A_{ij}^T \times x_j$$

$$\overline{x_4} = x'_4 + A_{44}^T \times x_4 + A_{45}^T \times x_5 + A_{46}^T \times x_6$$

$$\overline{x_5} = x'_5 + A_{54}^T \times \overline{x_4} + A_{55}^T \times x_5 + A_{56}^T \times x_6$$

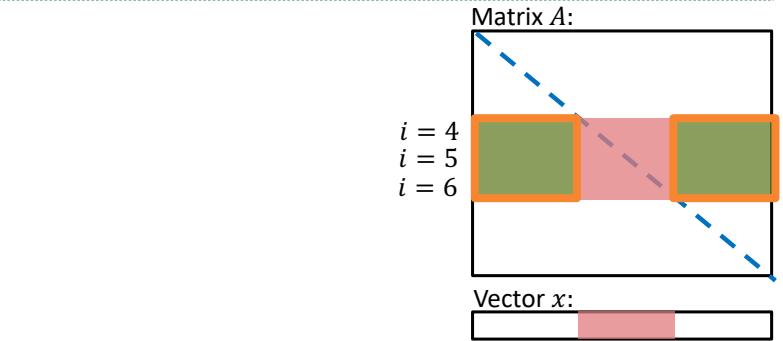
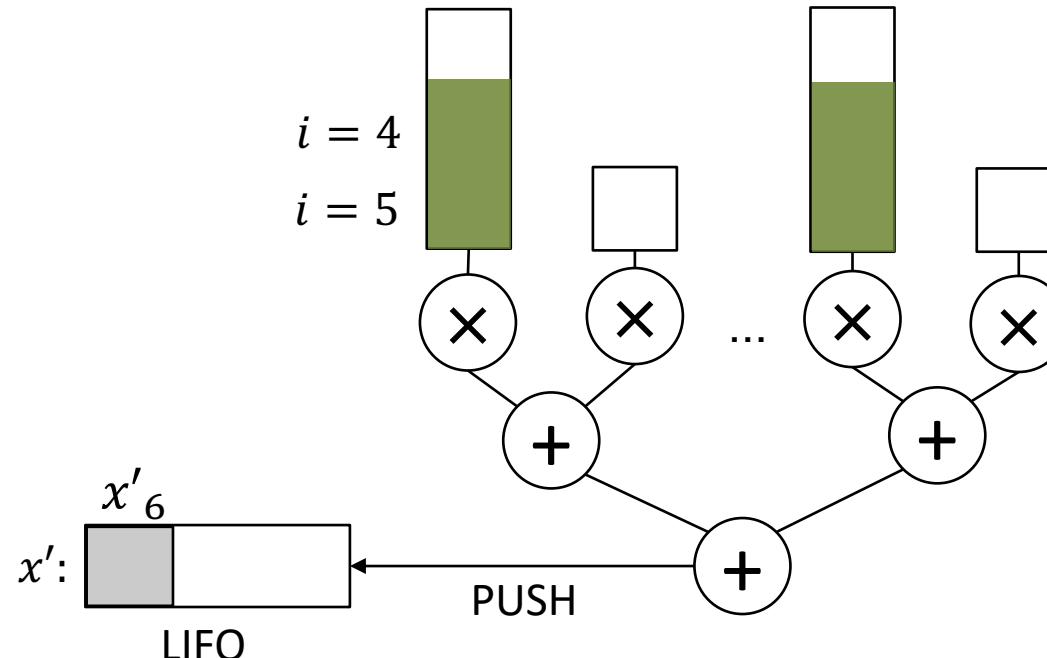
$$\overline{x_6} = x'_6 + A_{64}^T \times \overline{x_4} + A_{65}^T \times \overline{x_5} + A_{66}^T \times x_6$$



# Reordering the operations

39

- ▶ First, Alrescha
  - ▶ Executes the GEMV
  - ▶ Produces intermediate results (partial sum,  $x'$ )
  - ▶ Pushes  $x'$  into a LIFO to reuse them fast, later



$$x'_{\textcolor{orange}{i}} = \sum_{j \neq 4, 5, 6} A_{ij}^T \times x_j$$

$$\overline{x_4} = x'_{\textcolor{orange}{4}} + A_{44}^T \times x_4 + A_{45}^T \times x_5 + A_{46}^T \times x_6$$

$$\overline{x_5} = x'_{\textcolor{orange}{5}} + A_{54}^T \times \overline{x_4} + A_{55}^T \times x_5 + A_{56}^T \times x_6$$

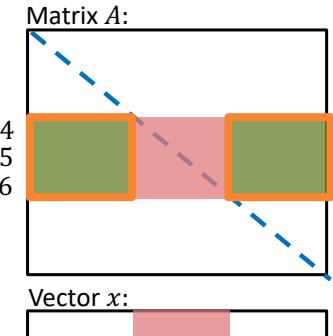
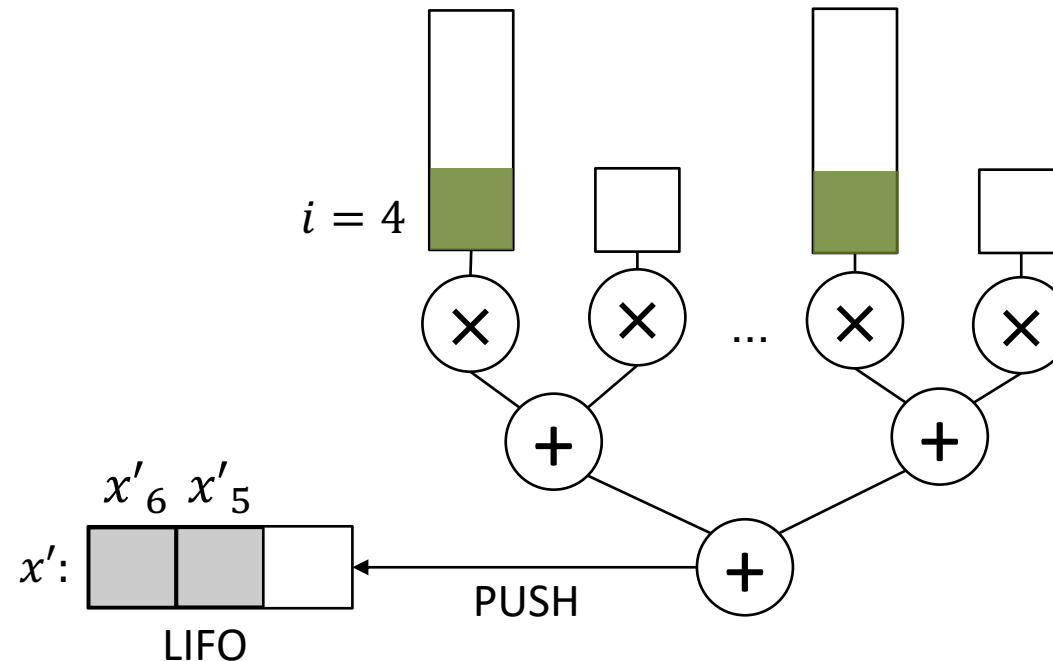
$$\overline{x_6} = x'_{\textcolor{orange}{6}} + A_{64}^T \times \overline{x_4} + A_{65}^T \times \overline{x_5} + A_{66}^T \times x_6$$



# Reordering the operations

40

- ▶ First, Alrescha
  - ▶ Executes the GEMV
  - ▶ Produces intermediate results (partial sum,  $x'$ )
  - ▶ Pushes  $x'$  into a LIFO to reuse them fast, later



$$x'_i = \sum_{j \neq 4, 5, 6} A_{ij}^T \times x_j$$

$$\overline{x_4} = x'_4 + A_{44}^T \times x_4 + A_{45}^T \times x_5 + A_{46}^T \times x_6$$

$$\overline{x_5} = x'_5 + A_{54}^T \times \overline{x_4} + A_{55}^T \times x_5 + A_{56}^T \times x_6$$

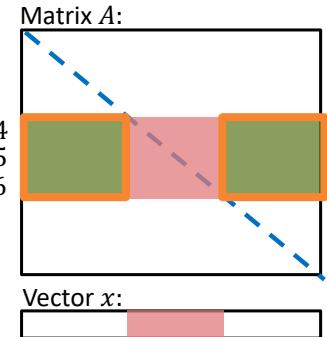
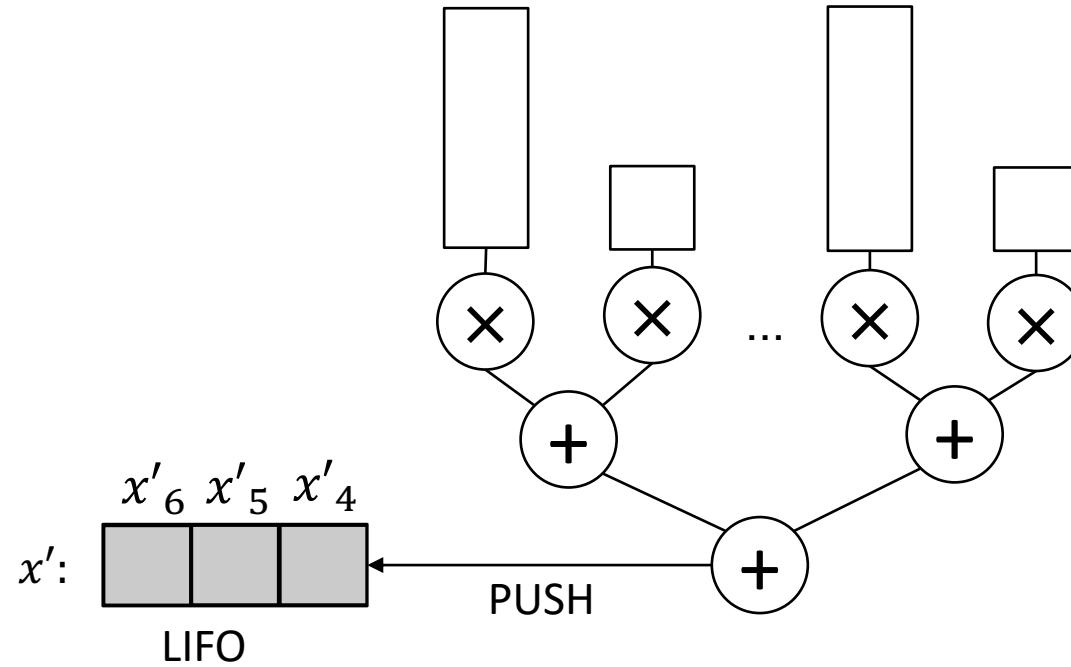
$$\overline{x_6} = x'_6 + A_{64}^T \times \overline{x_4} + A_{65}^T \times \overline{x_5} + A_{66}^T \times x_6$$



# Reordering the operations

41

- ▶ First, Alrescha
  - ▶ Executes the GEMV
  - ▶ Produces intermediate results (partial sum,  $x'$ )
  - ▶ Pushes  $x'$  into a LIFO to reuse them fast, later



$$x'_i = \sum_{j \neq 4, 5, 6} A_{ij}^T \times x_j$$

$$\overline{x_4} = x'_4 + A_{44}^T \times x_4 + A_{45}^T \times x_5 + A_{46}^T \times x_6$$

$$\overline{x_5} = x'_5 + A_{54}^T \times \overline{x_4} + A_{55}^T \times x_5 + A_{56}^T \times x_6$$

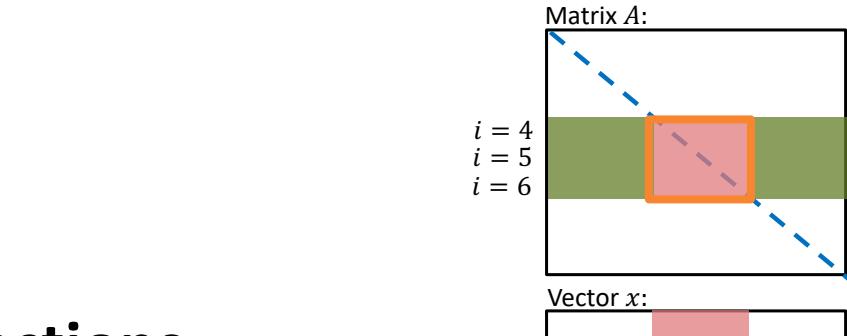
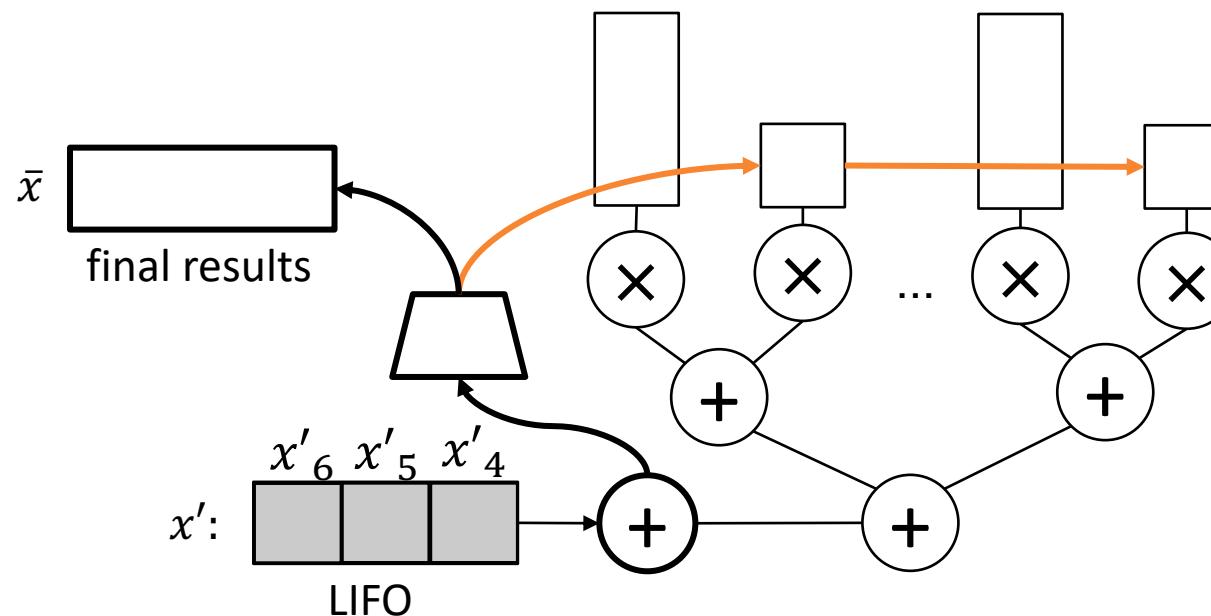
$$\overline{x_6} = x'_6 + A_{64}^T \times \overline{x_4} + A_{65}^T \times \overline{x_5} + A_{66}^T \times x_6$$



# Reordering the operations

42

- ▶ Then, Alrescha
  - ▶ Executes SymGS using **same reduction tree**
  - ▶ Pops  $x'$  from the LIFO to reuse them fast
  - ▶ **Reuses new  $\bar{x}$  immediately through shift connections**



$$x'_i = \sum_{j \neq 4, 5, 6} A_{ij}^T \times x_j$$

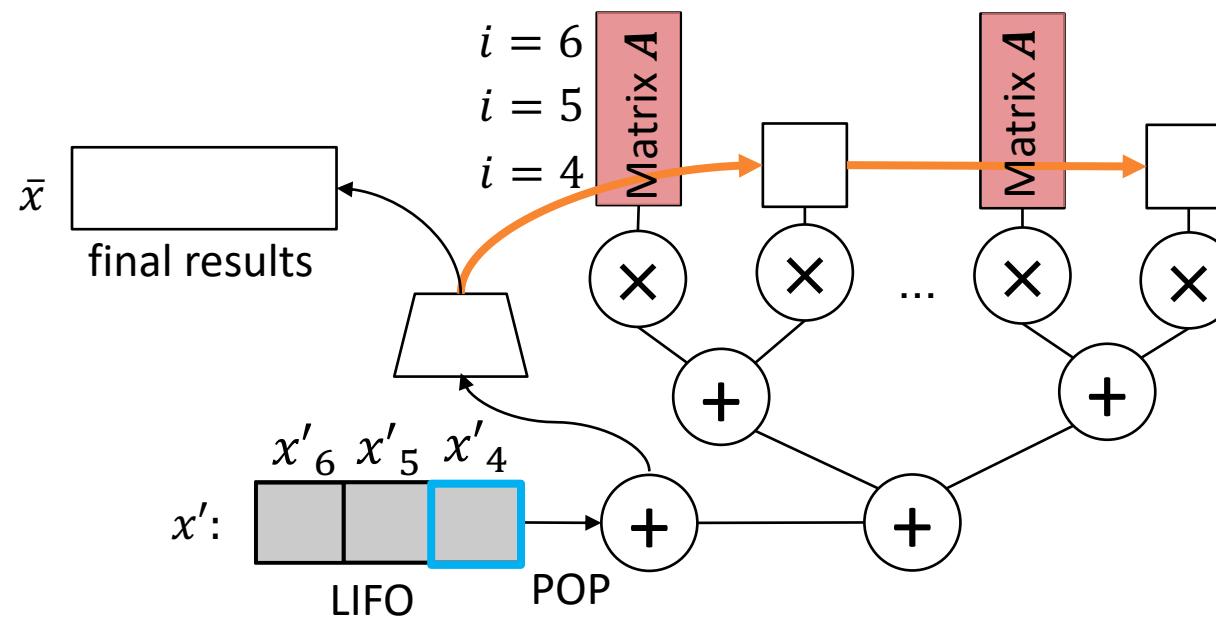
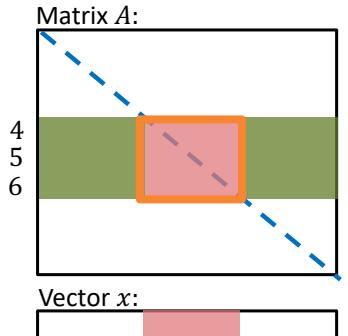
$$\begin{aligned} \bar{x}_4 &= x'_4 + A_{44}^T \times x_4 + A_{45}^T \times x_5 + A_{46}^T \times x_6 \\ \bar{x}_5 &= x'_5 + A_{54}^T \times \bar{x}_4 + A_{55}^T \times x_5 + A_{56}^T \times x_6 \\ \bar{x}_6 &= x'_6 + A_{64}^T \times \bar{x}_4 + A_{65}^T \times \bar{x}_5 + A_{66}^T \times x_6 \end{aligned}$$



# Reordering the operations

43

- ▶ Then, Alrescha
  - ▶ Executes SymGS using **same reduction tree**
  - ▶ Pops  $x'$  from the LIFO to reuse them fast
  - ▶ **Reuses new  $\bar{x}$  immediately through shift connections**



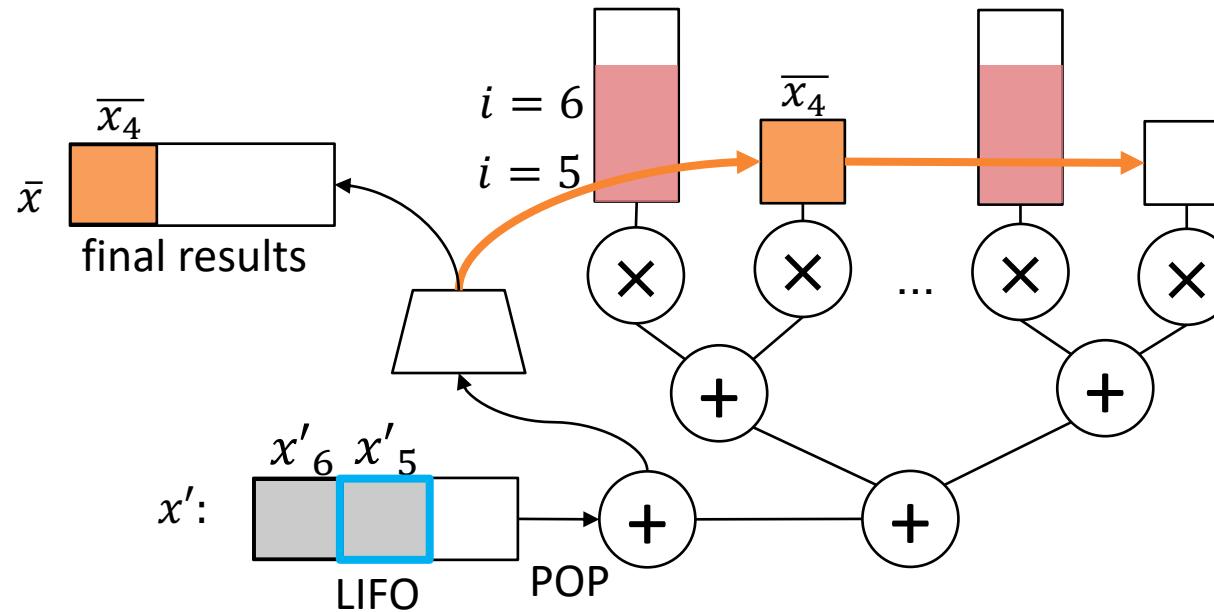
$$\begin{aligned} x'_i &= \sum_{j \neq 4, 5, 6} A_{ij}^T \times x_j \\ \bar{x}_4 &= x'_4 + A_{44}^T \times x_4 + A_{45}^T \times x_5 + A_{46}^T \times x_6 \\ \bar{x}_5 &= x'_5 + A_{54}^T \times \bar{x}_4 + A_{55}^T \times x_5 + A_{56}^T \times x_6 \\ \bar{x}_6 &= x'_6 + A_{64}^T \times \bar{x}_4 + A_{65}^T \times \bar{x}_5 + A_{66}^T \times x_6 \end{aligned}$$



# Reordering the operations

44

- ▶ Then, Alrescha
  - ▶ Executes SymGS using **same reduction tree**
  - ▶ Pops  $x'$  from the LIFO to reuse them fast
  - ▶ **Reuses new  $\bar{x}$  immediately through shift connections**



Matrix  $A$ :

			i = 4	i = 5	i = 6

Vector  $x$ :

--	--	--	--	--	--

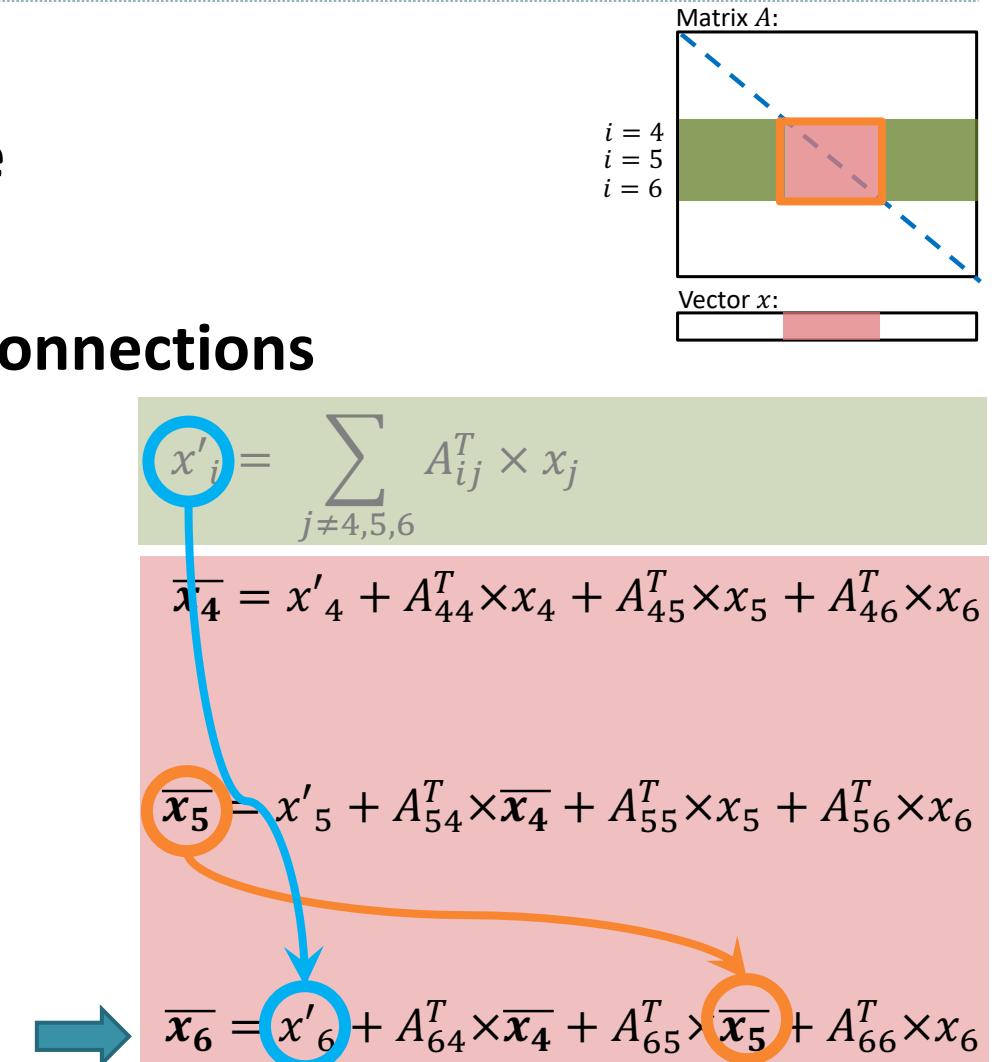
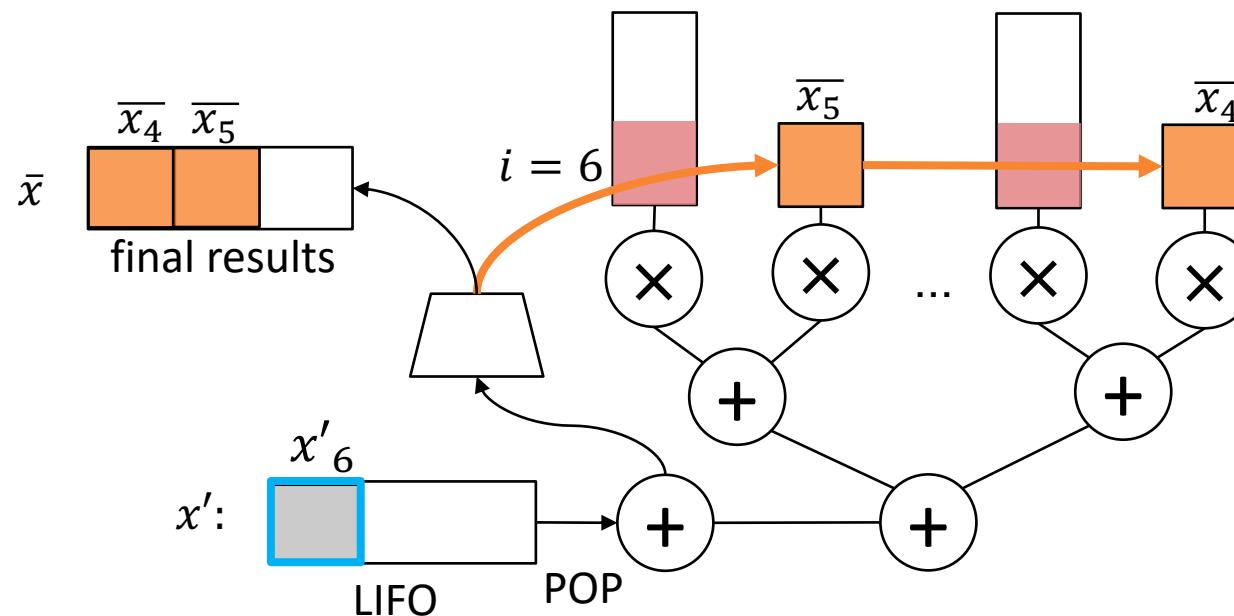
$$\bar{x}_i = \sum_{j \neq 4, 5, 6} A_{ij}^T \times x_j$$
$$\bar{x}_4 = x'_4 + A_{44}^T \times x_4 + A_{45}^T \times x_5 + A_{46}^T \times x_6$$
$$\bar{x}_5 = x'_5 + A_{54}^T \times \bar{x}_4 + A_{55}^T \times x_5 + A_{56}^T \times x_6$$
$$\bar{x}_6 = x'_6 + A_{64}^T \times \bar{x}_4 + A_{65}^T \times \bar{x}_5 + A_{66}^T \times x_6$$



# Reordering the operations

45

- ▶ Then, Alrescha
  - ▶ Executes SymGS using **same reduction tree**
  - ▶ Pops  $x'$  from the LIFO to reuse them fast
  - ▶ **Reuses new  $\bar{x}$  immediately through shift connections**

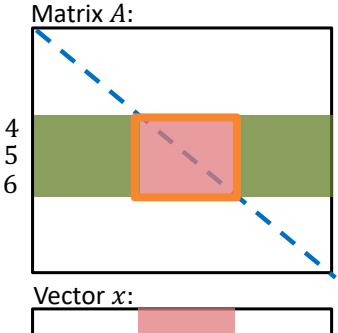
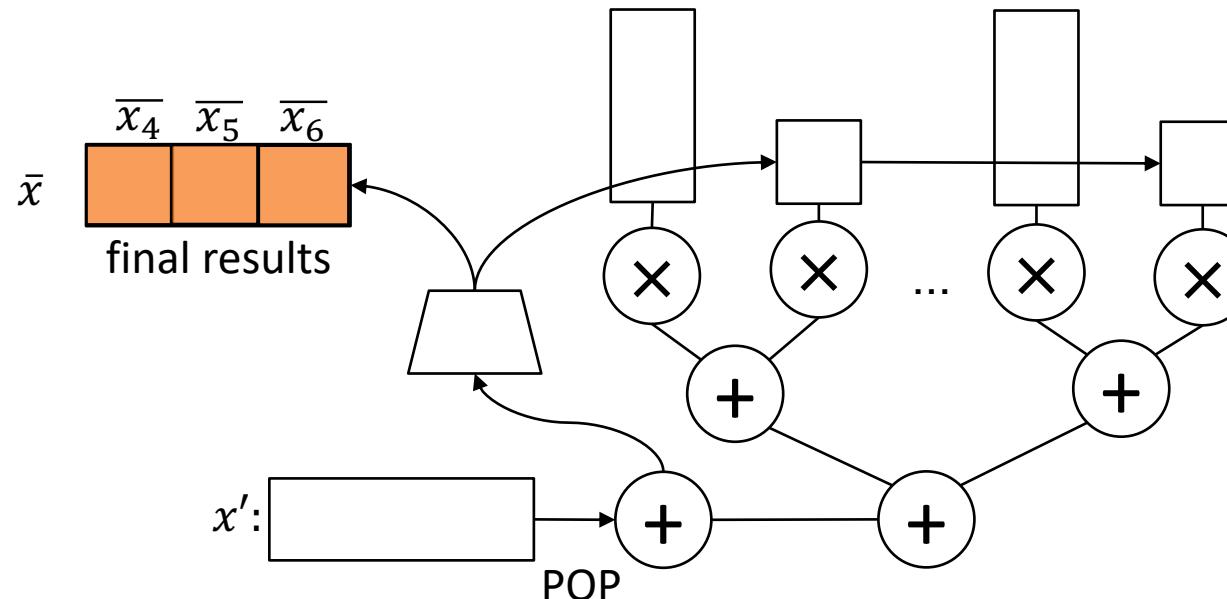




# Reordering the operations

46

- ▶ Then, Alrescha
  - ▶ Executes SymGS using **same reduction tree**
  - ▶ Pops  $x'$  from the LIFO to reuse them fast
  - ▶ **Reuses new  $\bar{x}$  immediately through shift connections**



$$\bar{x}_i = \sum_{j \neq 4, 5, 6} A_{ij}^T \times x_j$$

$$\bar{x}_4 = x'_4 + A_{44}^T \times x_4 + A_{45}^T \times x_5 + A_{46}^T \times x_6$$

$$\bar{x}_5 = x'_5 + A_{54}^T \times \bar{x}_4 + A_{55}^T \times x_5 + A_{56}^T \times x_6$$

$$\bar{x}_6 = x'_6 + A_{64}^T \times \bar{x}_4 + A_{65}^T \times \bar{x}_5 + A_{66}^T \times x_6$$

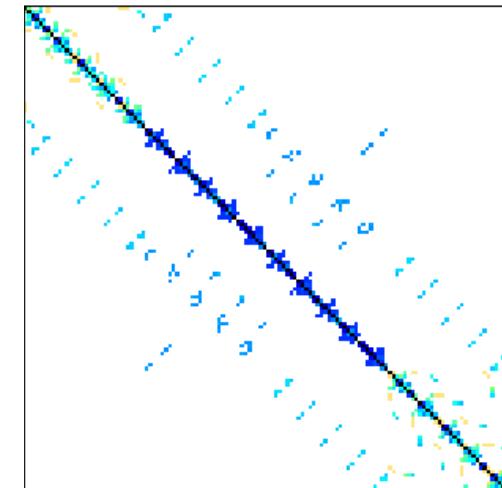
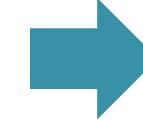
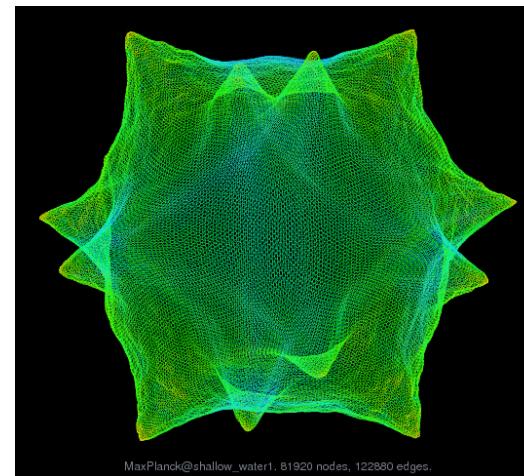
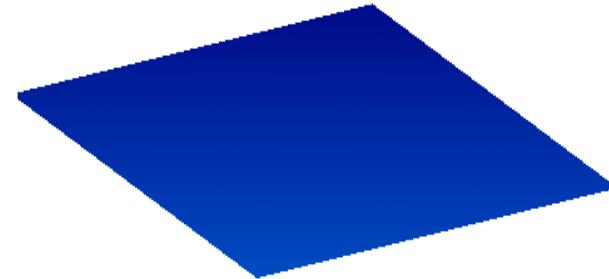


# Putting them together for **sparse** matrices

47

What: Matrix  $A$  in  $Ax = b$

Why: Not all the points in a 3D-grid are occupied



Shallow-water equations<sup>1</sup>  
(a set of PDEs)

Discretized to a 3D grid <sup>2</sup>

Matrix  $A$

<sup>1</sup>[https://en.wikipedia.org/wiki/Shallow\\_water\\_equations](https://en.wikipedia.org/wiki/Shallow_water_equations)

<sup>2</sup> From Max-Plank Institute of Meteorology



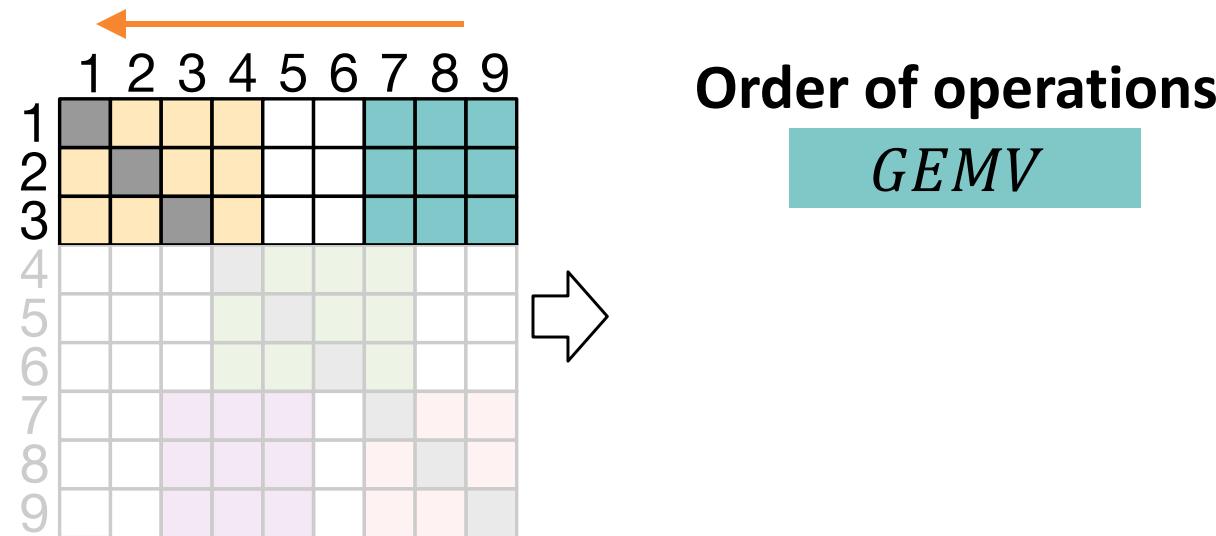
# Putting them together for **sparse** matrices

48

Alrescha accesses the vector  $x$  from cache (1KB)

Alrescha **streams** non-zero blocks<sup>1</sup> of matrix  $A$ :

- ▶ First,  $GEMV$  non-diagonals blocks
- ▶ Then,  $SymGS$  on diagonal blocks



<sup>1</sup> As shown in prior work, the target scientific problems have block structure.



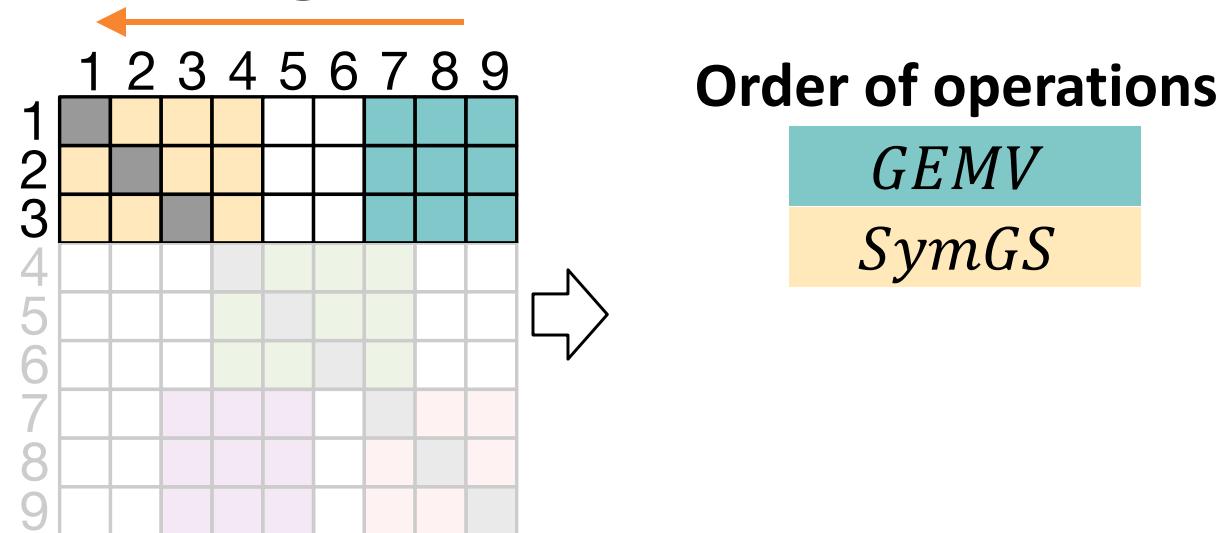
# Putting them together for **sparse** matrices

49

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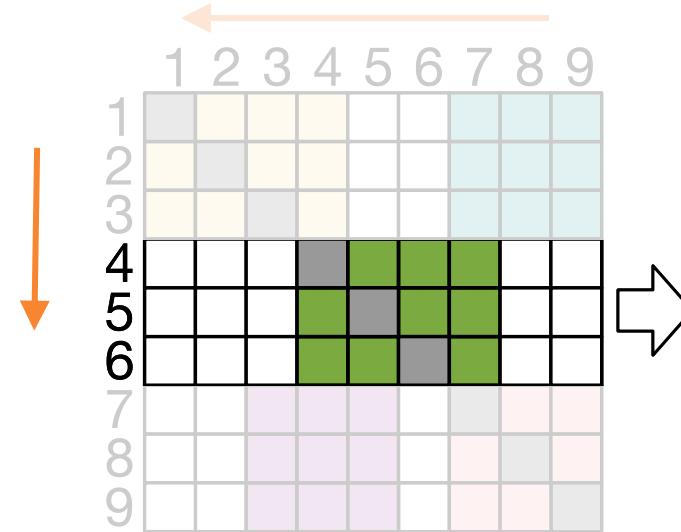
# Putting them together for **sparse** matrices

50

Alrescha accesses the vector  $x$  from cache (1KB)

Alrescha **streams** non-zero blocks<sup>1</sup> of matrix  $A$ :

- ▶ First,  $GEMV$  non-diagonals blocks
- ▶ Then,  $SymGS$  on diagonal blocks



## Order of operations

$GEMV$
$SymGS$
$SymGS$

<sup>1</sup> As shown in prior work, the target scientific problems have block structure.



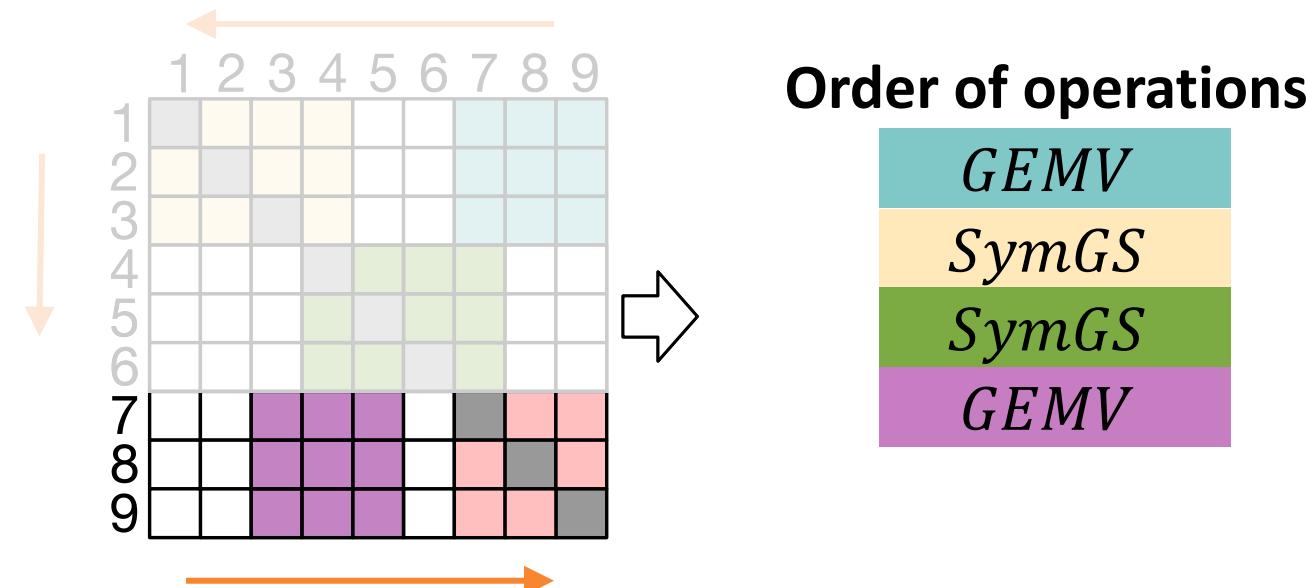
# Putting them together for **sparse** matrices

51

Alrescha accesses the vector  $x$  from cache (1KB)

Alrescha **streams** non-zero blocks<sup>1</sup> of matrix  $A$ :

- ▶ First, *GEMV* non-diagonals blocks
- ▶ Then, *SymGS* on diagonal blocks



<sup>1</sup> As shown in prior work, the target scientific problems have block structure.



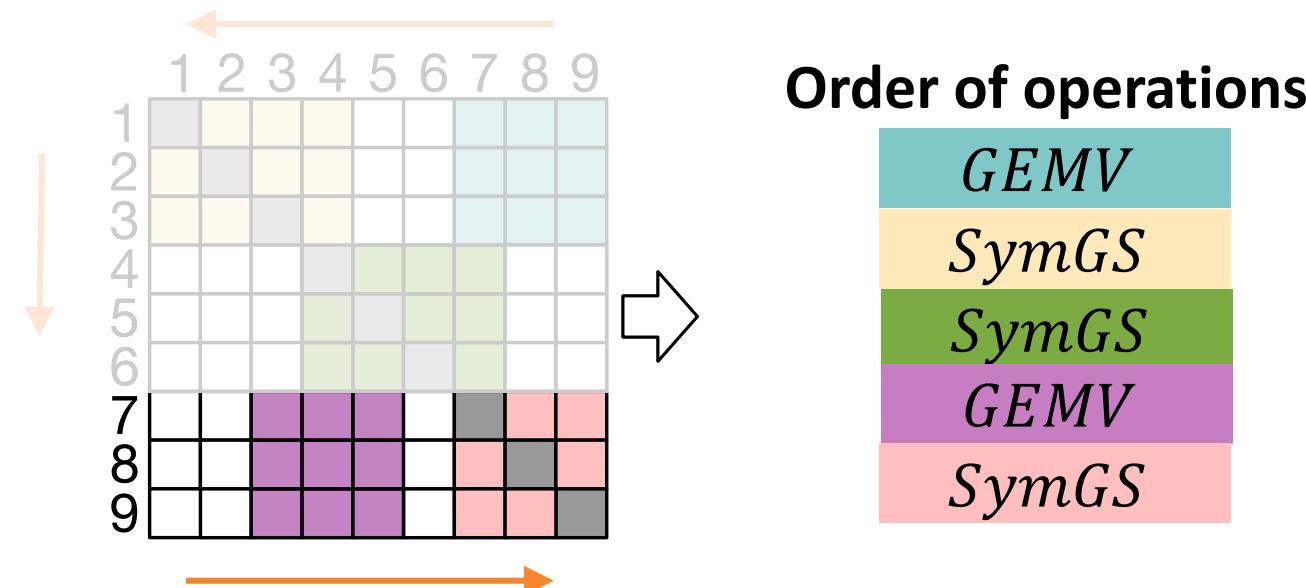
# Putting them together for **sparse** matrices

52

Alrescha accesses the vector  $x$  from cache (1KB)

Alrescha **streams** non-zero blocks<sup>1</sup> of matrix  $A$ :

- ▶ First,  $GEMV$  non-diagonals blocks
- ▶ Then,  $SymGS$  on diagonal blocks



<sup>1</sup> As shown in prior work, the target scientific problems have block structure.



# Outline

53

- ▶ Using PDEs for modeling and key challenges
- ▶ **Alrescha**
  - ▶ Main contributions
  - ▶ **Storage format**
  - ▶ Reconfigurable microarchitecture
  - ▶ Broad applications
- ▶ Results
- ▶ Conclusions

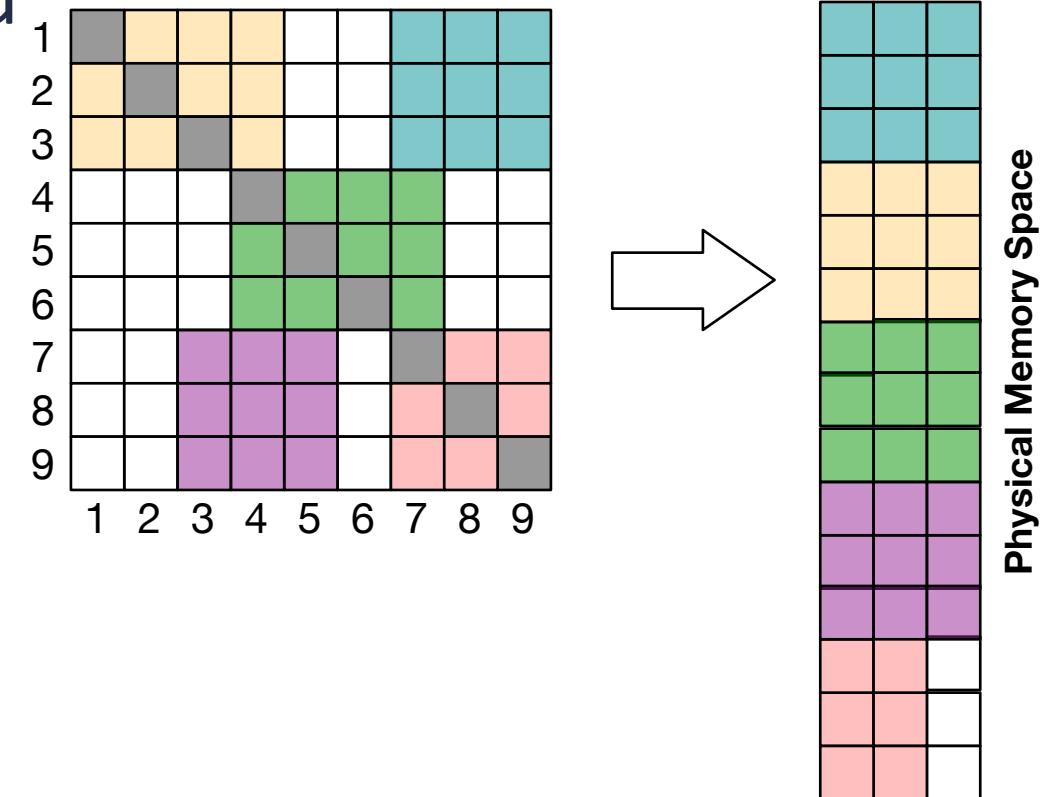


# Storage format

54

Similar to BCSR<sup>1</sup> with linear overhead

- ▶ Order of blocks:
  - ▶ Same as order of operations



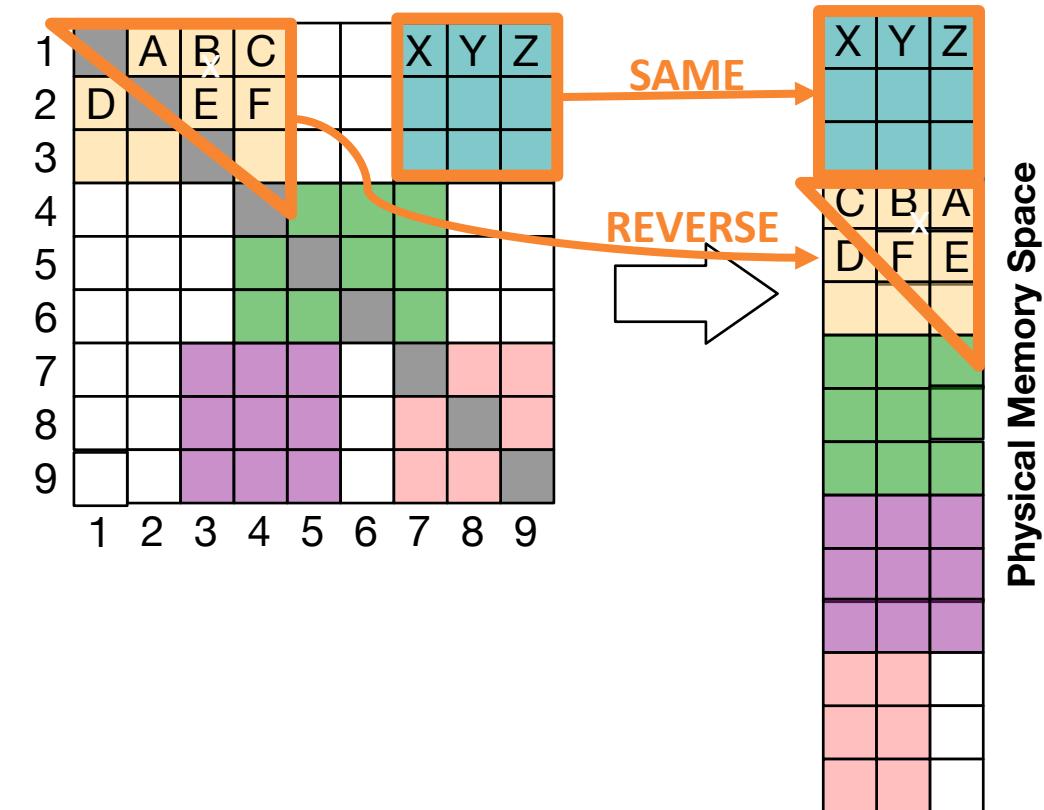


# Storage format

55

Similar to BCSR<sup>1</sup> with linear overhead

- ▶ Order of blocks:
  - ▶ Same as order of operations
- ▶ Order of elements:
  - ▶ Non-diagonal blocks: original
  - ▶ Up triangle of diagonal blocks: reverse



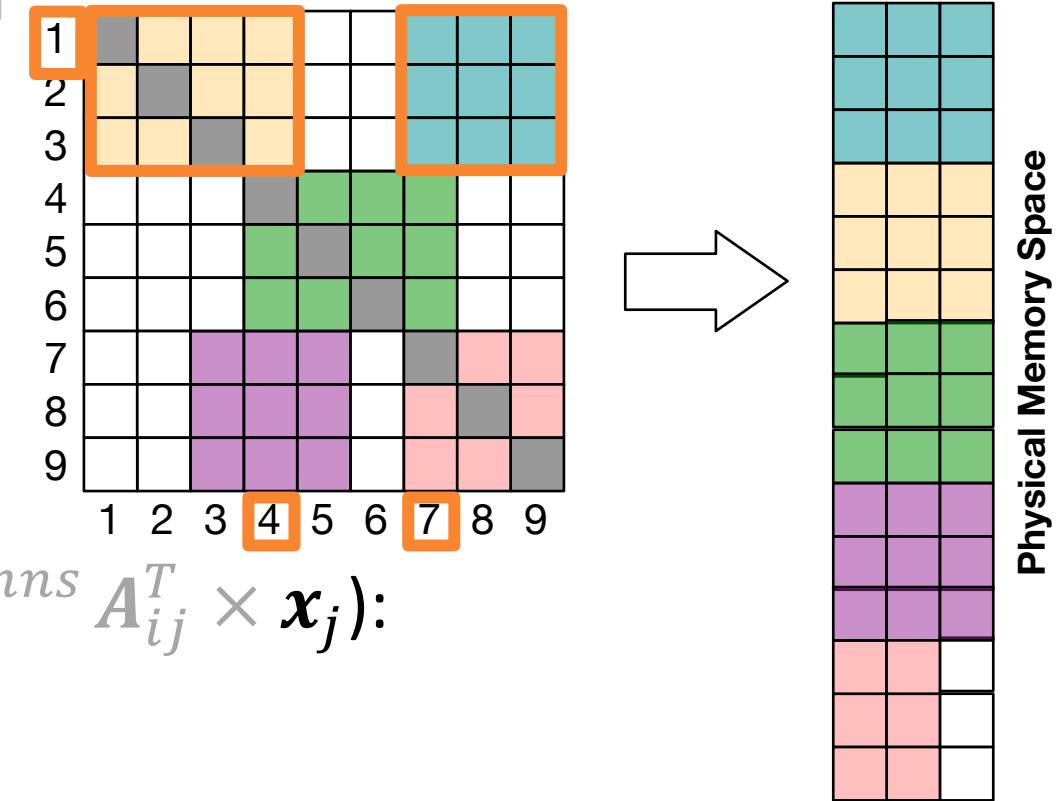


# Storage format

56

Similar to BCSR<sup>1</sup> with linear overhead

- ▶ Order of blocks:
  - ▶ Same as order of operations
- ▶ Order of elements:
  - ▶ Non-diagonal blocks: original
  - ▶ Up triangle of diagonal blocks: reverse
- ▶ Indexing (for cache access  $x_i = \sum_{j=0}^{\text{columns}} A_{ij}^T \times x_j$ ):
  - ▶ Input indices: 7, 4,
  - ▶ Output indices: 1,



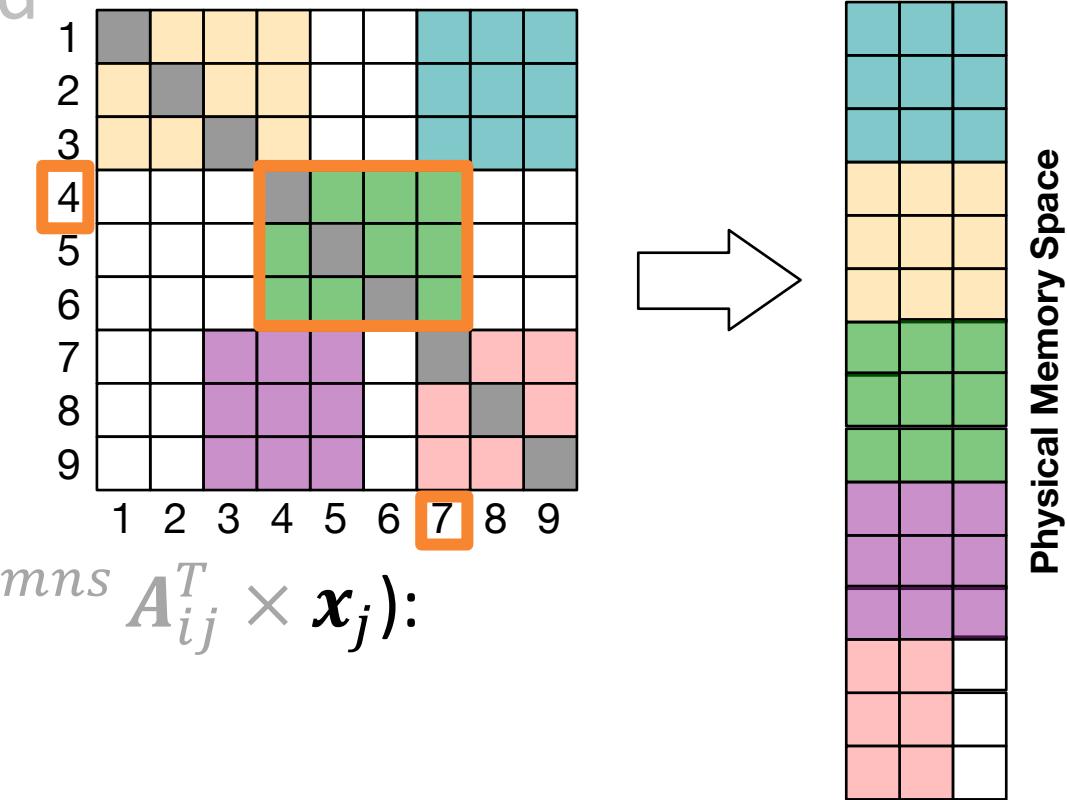


# Storage format

57

Similar to BCSR<sup>1</sup> with linear overhead

- ▶ Order of blocks:
  - ▶ Same as order of operations
- ▶ Order of elements:
  - ▶ Non-diagonal blocks: original
  - ▶ Up triangle of diagonal blocks: reverse
- ▶ Indexing (for cache access  $x_i = \sum_{j=0}^{\text{columns}} A_{ij}^T \times x_j$ ):
  - ▶ Input indices: 7, 4, 7,
  - ▶ Output indices: 1, 4,



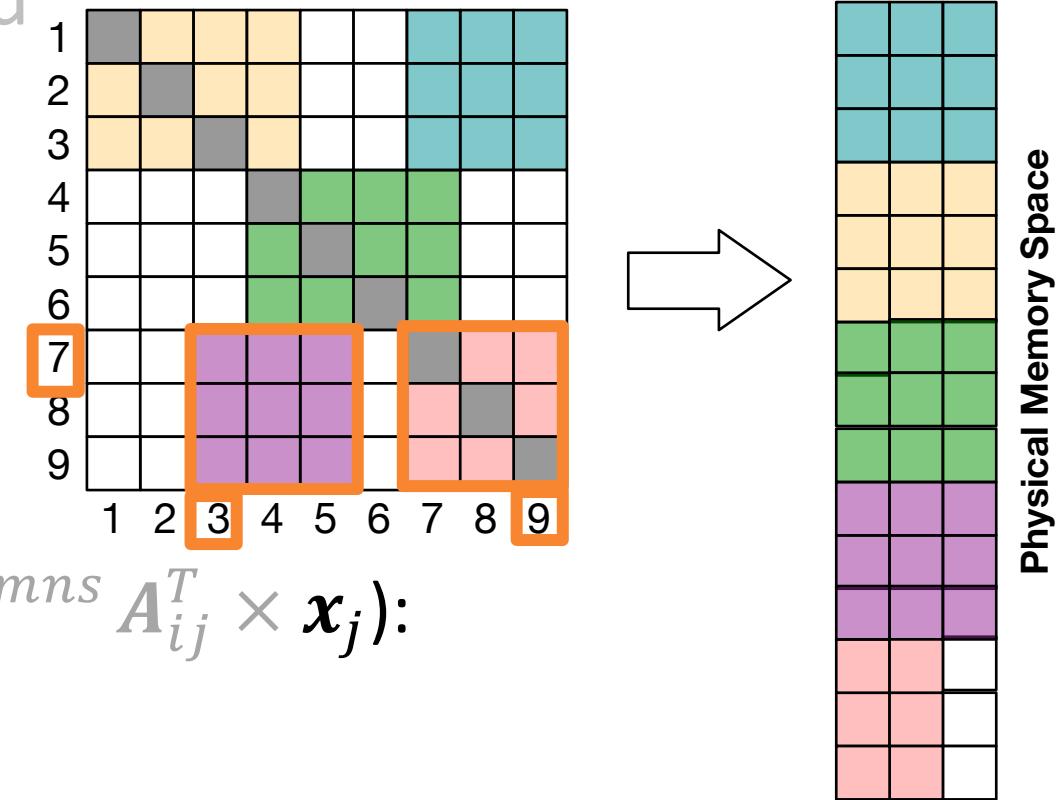


# Storage format

58

Similar to BCSR<sup>1</sup> with linear overhead

- ▶ Order of blocks:
  - ▶ Same as order of operations
- ▶ Order of elements:
  - ▶ Non-diagonal blocks: original
  - ▶ Up triangle of diagonal blocks: reverse
- ▶ Indexing (for cache access  $x_i = \sum_{j=0}^{\text{columns}} A_{ij}^T \times x_j$ ):
  - ▶ Input indices: 7, 4, 7, 3, 9
  - ▶ Output indices: 1, 4, 7





# Outline

59

- ▶ Using PDEs for modeling and key challenges
- ▶ **Alrescha**
  - ▶ Main contributions
  - ▶ Storage format
  - ▶ **Reconfigurable microarchitecture**
  - ▶ Broad applications
- ▶ Results
- ▶ Conclusions

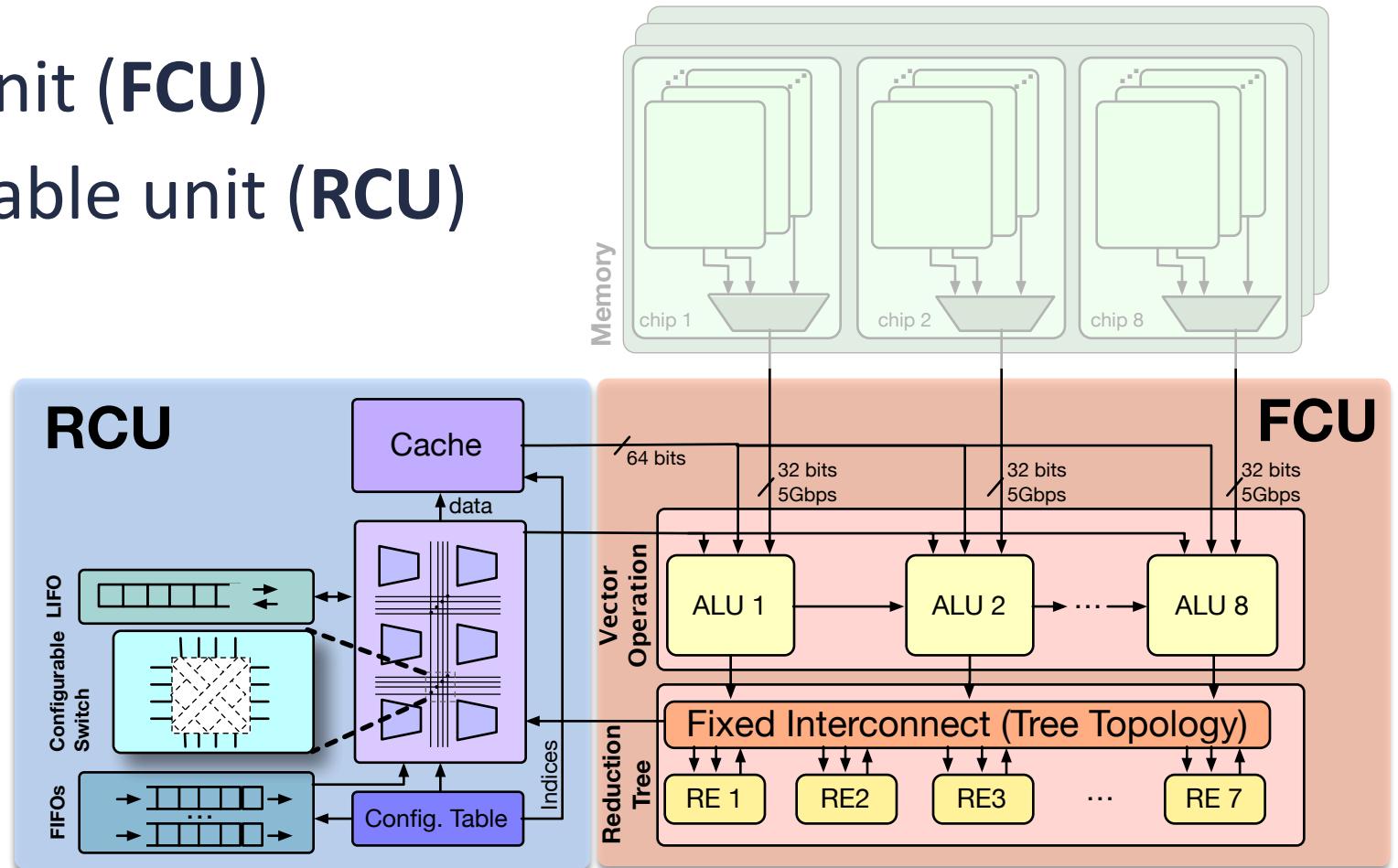


# Lightweight reconfigurable microarchitecture

60

Alrescha includes:

- ▶ A fixed compute unit (**FCU**)
- ▶ A small reconfigurable unit (**RCU**)

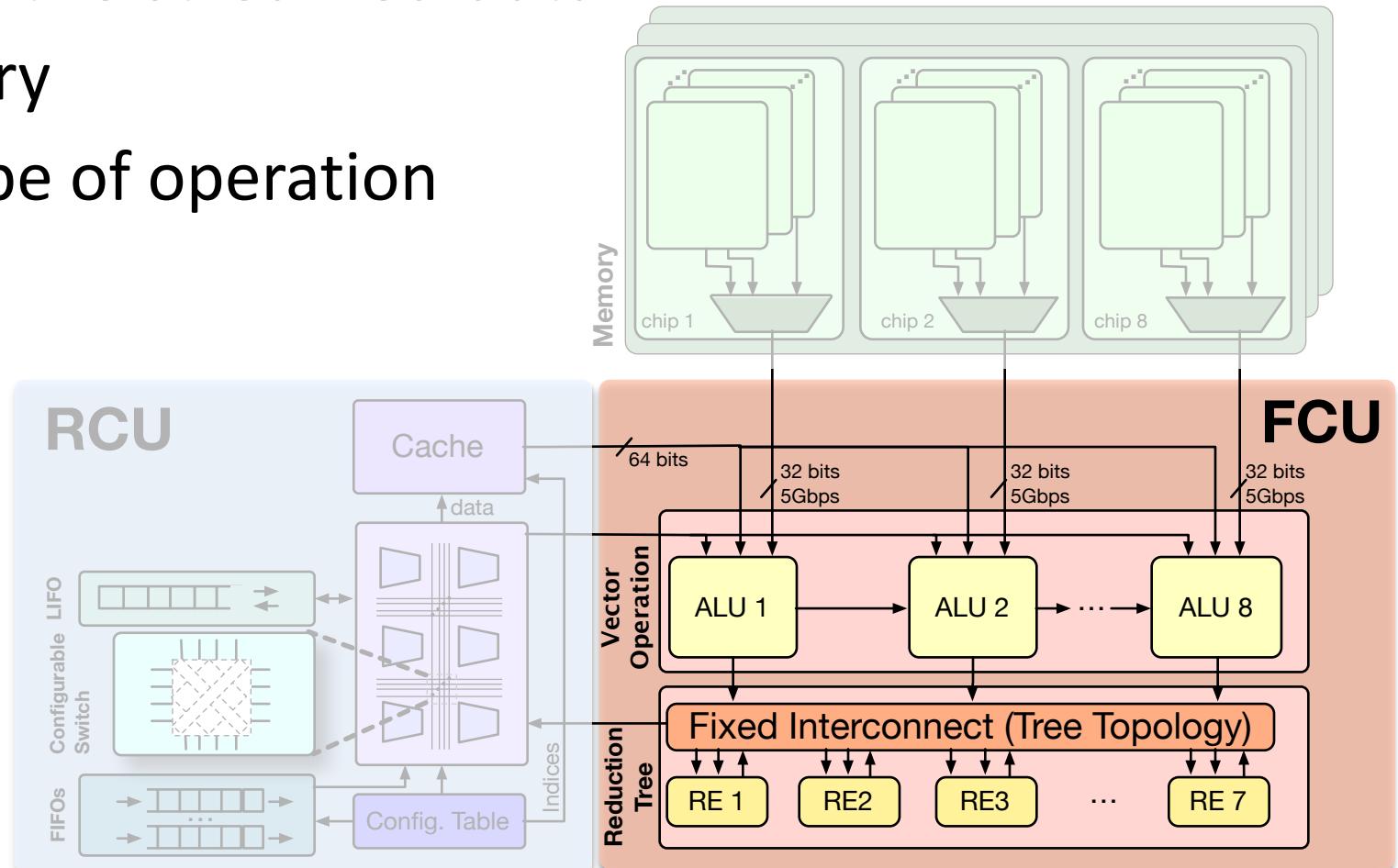




# Fixed compute unit (FCU)

61

- ▶ Applies reduction on the streamed data
  - ▶ Directly from memory
  - ▶ Regardless of the type of operation

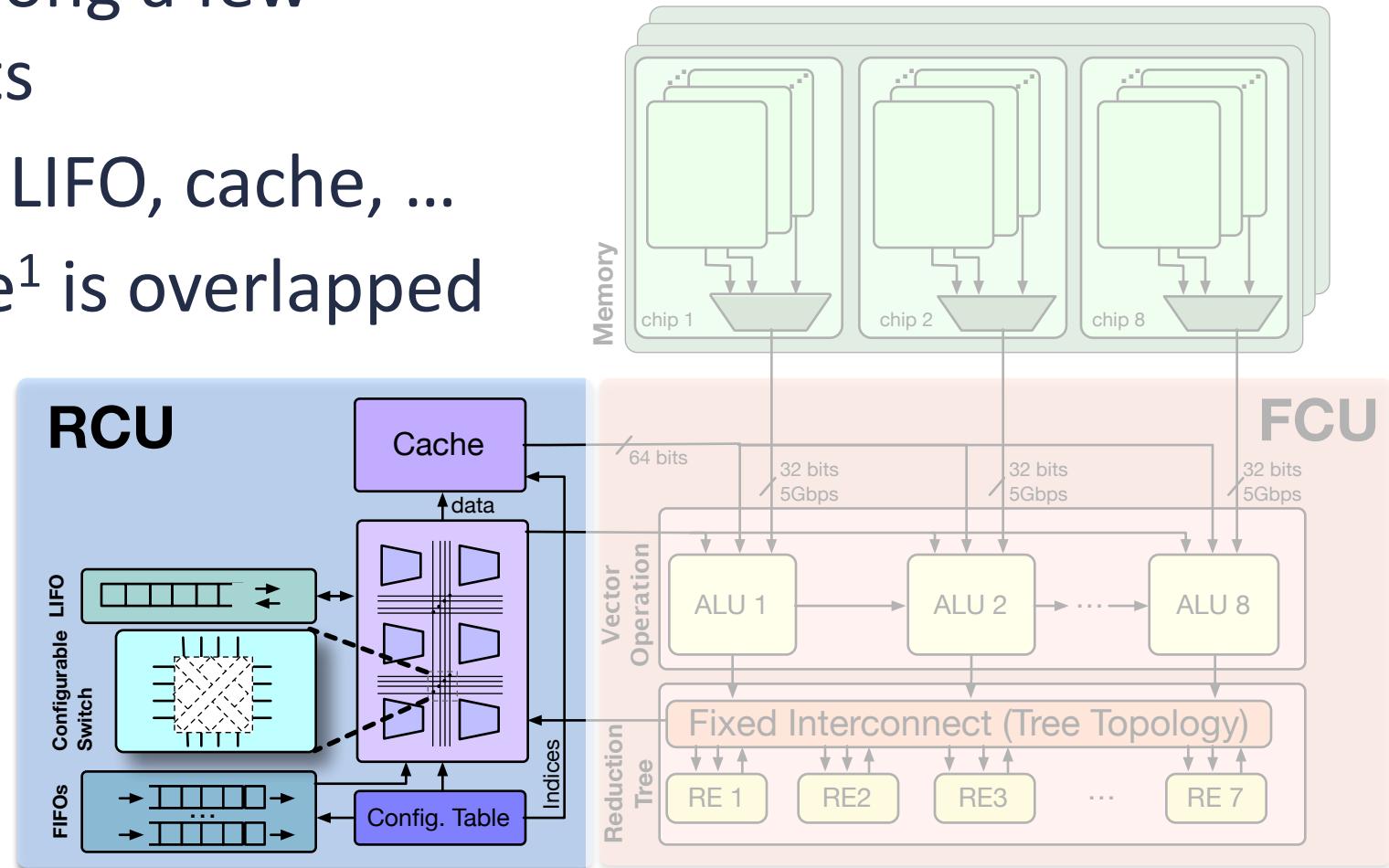




# Reconfigurable compute unit (RCU)

62

- ▶ Interconnections among a few simple compute units
- ▶ Connections: FCU -> LIFO, cache, ...
- ▶ Reconfiguration time<sup>1</sup> is overlapped with draining FCU
- ▶ Small and fast in both ASIC/FPGA

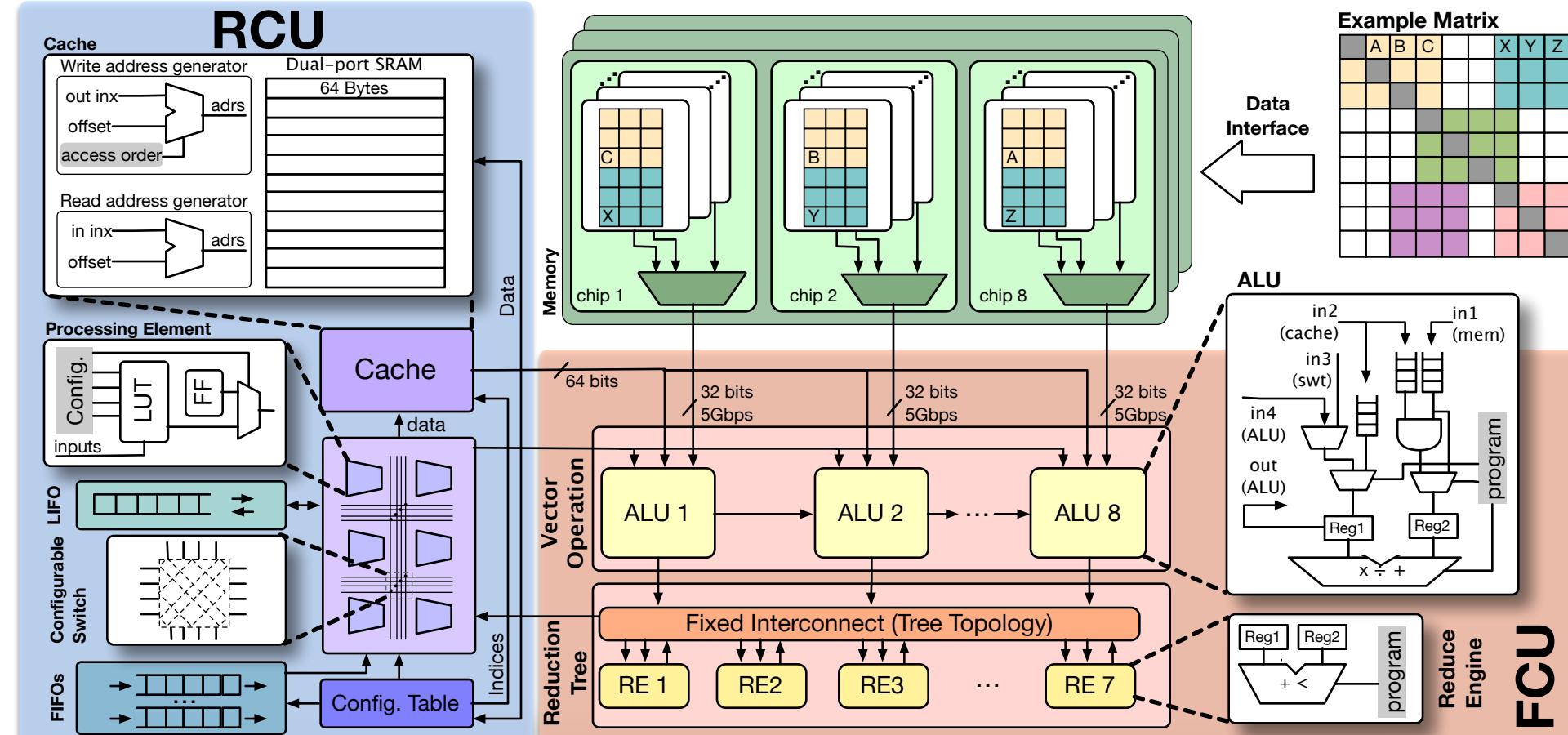


<sup>1</sup>Based on Xilinx Virtex-4 numbers using 90nm technology, it takes ~0.3 ns



# Lightweight reconfigurable microarchitecture

63



For more details please refer to paper



# Outline

64

- ▶ Using PDEs for modeling and key challenges
- ▶ **Alrescha**
  - ▶ Main contributions
  - ▶ Storage format
  - ▶ Reconfigurable microarchitecture
  - ▶ **Broad applications**
- ▶ Results
- ▶ Conclusions



# Broad Applications

65

Alrescha accelerates **other sparse algorithms**, because of

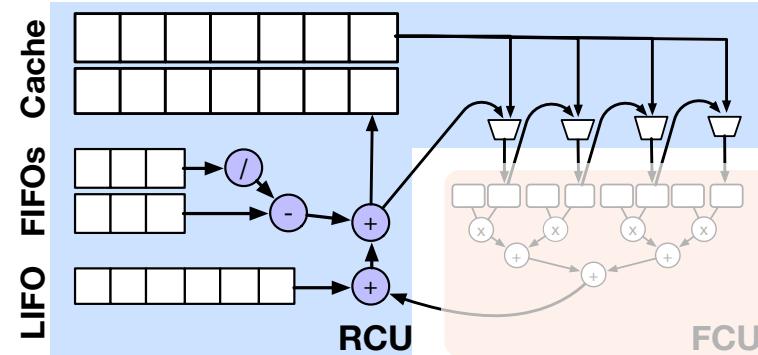
- ▶ The common reduction engine
- ▶ The lightweight (partial) reconfigurable microarchitecture

<sup>1</sup> SpMV: Sparse matrix vector multiplication

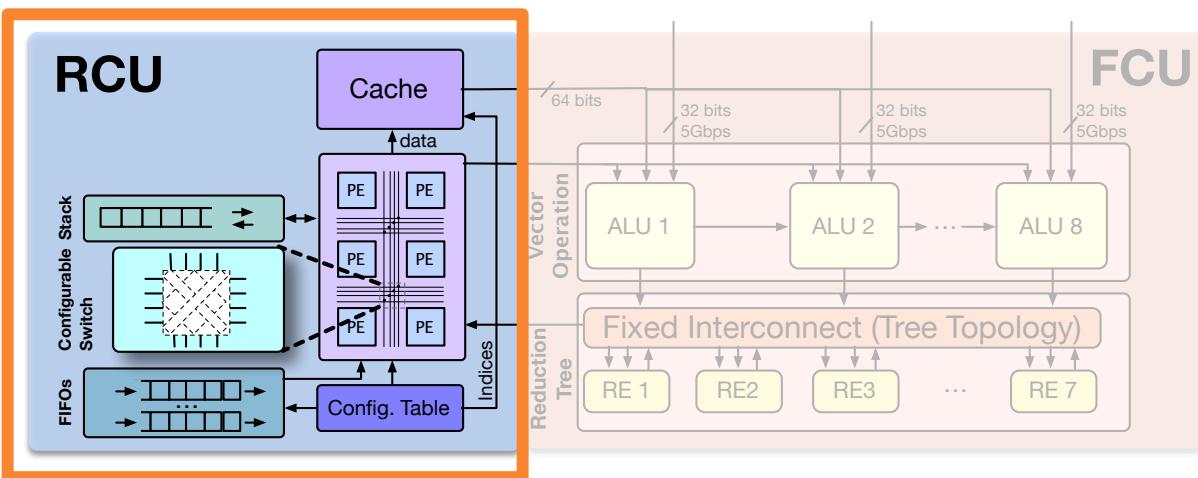


# Broad Applications

66



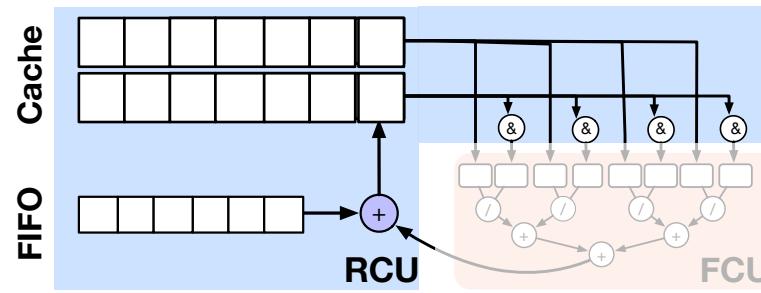
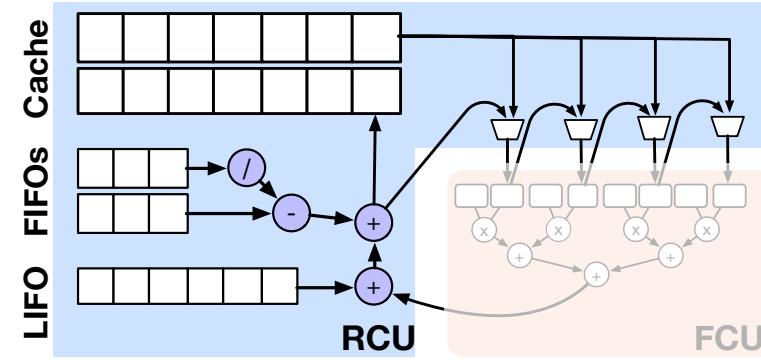
PDE Solver



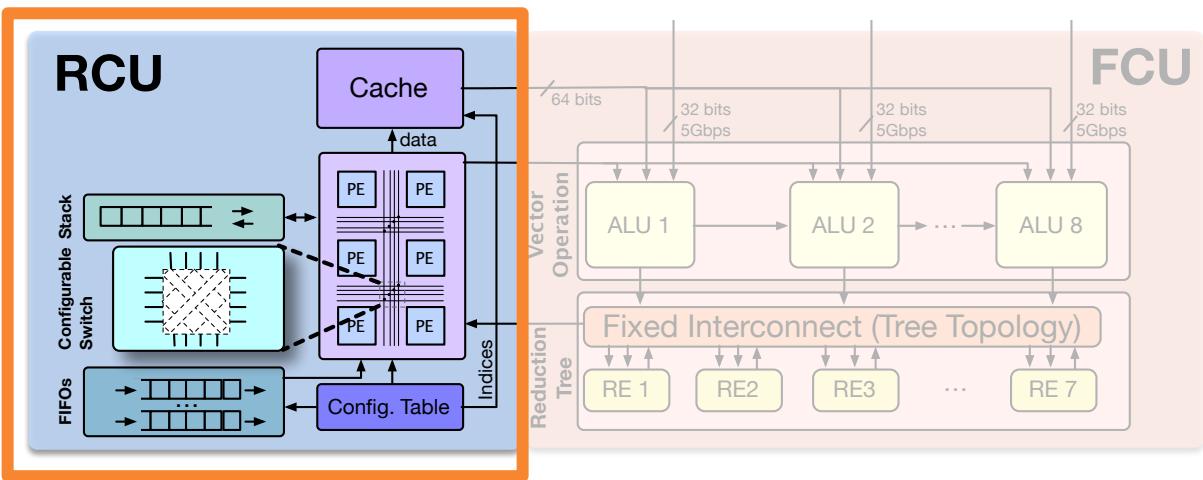


# Broad Applications

67



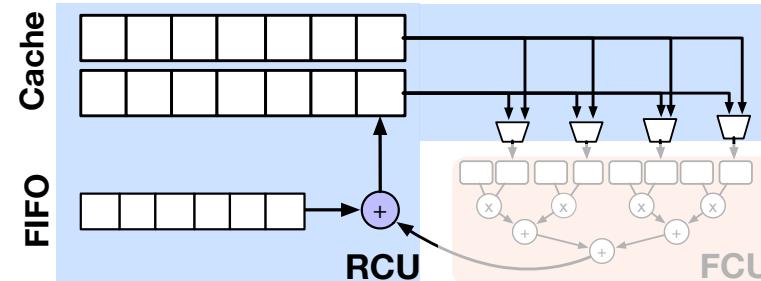
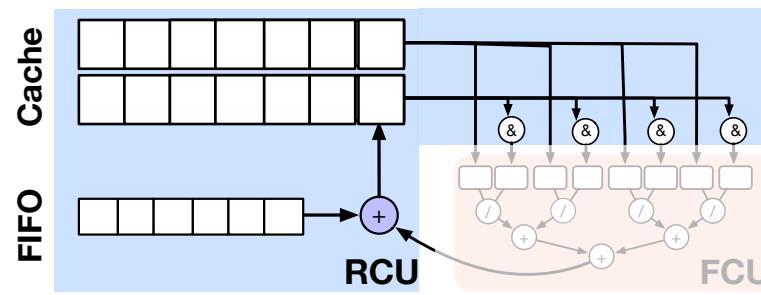
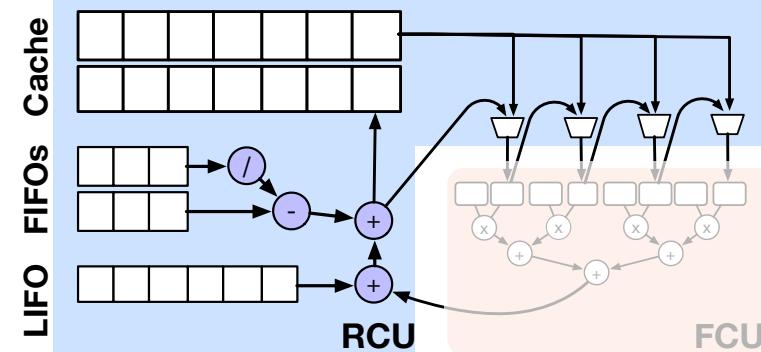
PDE Solver  
PageRank





# Broad Applications

68

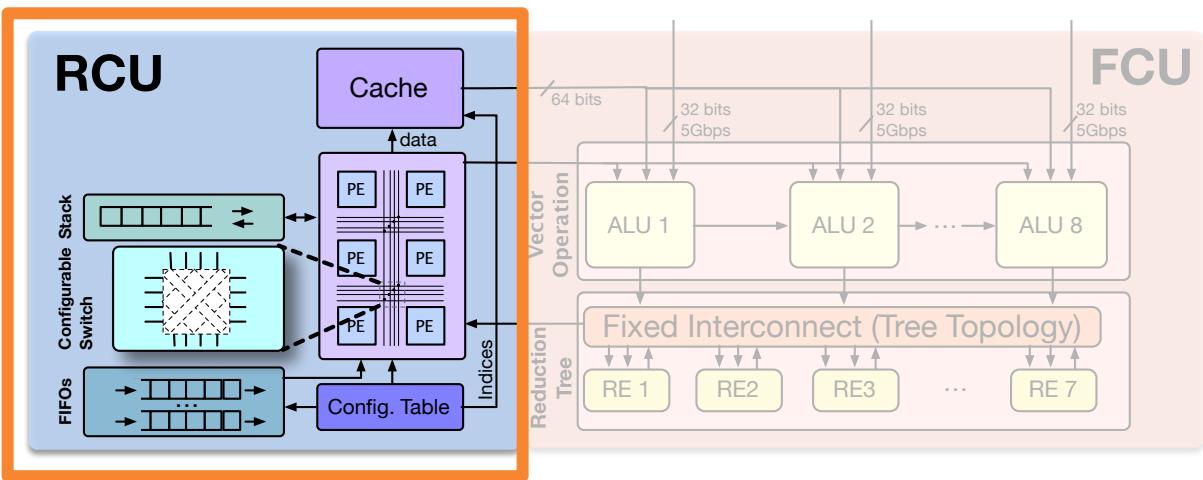


PDE Solver

PageRank

SpMV<sup>1</sup>

BFS<sup>2</sup>



<sup>1</sup> SpMV: Sparse matrix-vector multiplication

<sup>2</sup> BFS: Breadth-first search

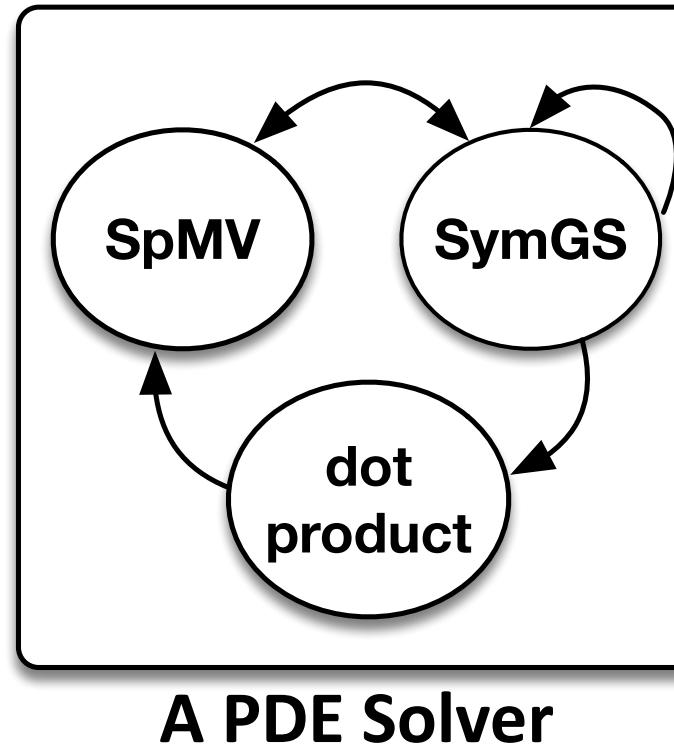


# Broad Applications

69

Alrescha is the first multi-kernel sparse accelerator

- ▶ Problems including different kernels (e.g., SpMV and SymGS)





# Outline

70

- ▶ Using PDEs for modeling and key challenges
- ▶ Alrescha
  - ▶ Main contributions
  - ▶ Storage format
  - ▶ Reconfigurable microarchitecture
  - ▶ Broad applications
- ▶ **Results**
- ▶ Conclusions



# Experimental Setup

71

- ▶ Implementation:
  - ▶ Preprocessing: Matlab
  - ▶ Simulation: Cycle-accurate C++ simulator
- ▶ Benchmarks
  - ▶ Algorithms: PCG, SpMV, BFS, SSSP, PageRank
  - ▶ Datasets: Sparse matrices from SuiteSparse collection<sup>1</sup>
- ▶ Baselines
  - ▶ CPU: Intel Xeon E5
  - ▶ GPU: NVIDIA Tesla K40c
  - ▶ State-of-the-art accelerators: Memristive<sup>2</sup>, OuterSPACE<sup>3</sup>, GraphR<sup>4</sup>
  - ▶ Memory bandwidth is similar among comparisons

<sup>1</sup><https://sparse.tamu.edu/>

<sup>2</sup>B. Feinberg et al. ISCA'18

<sup>3</sup>S. Pal, et al. HPCA'18

<sup>4</sup>L. Son, et al. HPCA'18

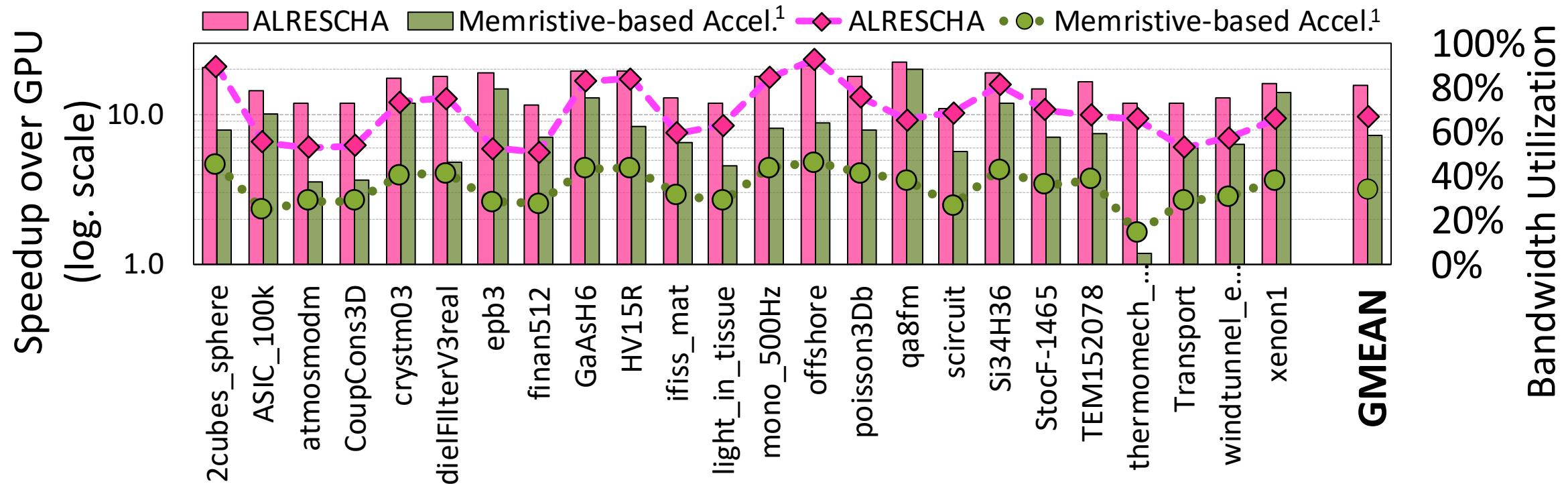


# Speedup for scientific workloads

72

Alrescha resolves performance bottleneck of PDE solvers

- ▶ 2.1x speedup compared to emerging technologies
- ▶ 15.6x speedup over GPU



<sup>1</sup>B. Feinberg et al. "Enabling scientific computing on memristive accelerators," ISCA'18

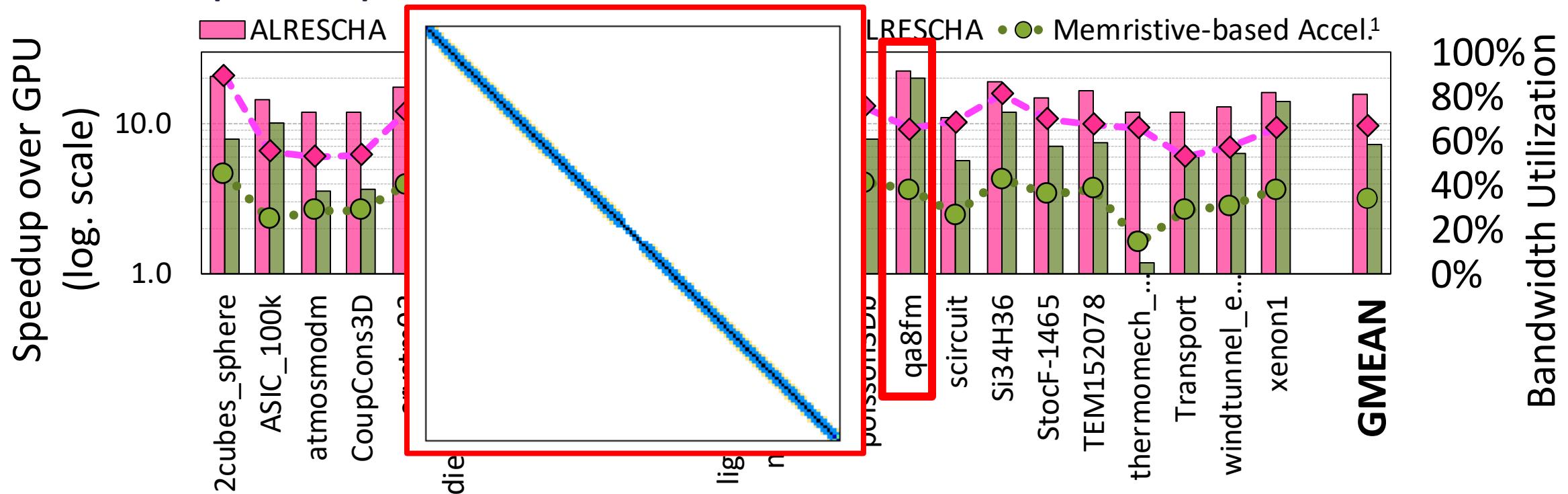


# Speedup for scientific workloads

73

Alrescha resolves performance bottleneck

- ▶ 2.1x speedup compared to emerging technologies
- ▶ 15.6x speedup over GPU



<sup>1</sup>B. Feinberg et al. "Enabling scientific computing on memristive accelerators," ISCA'18

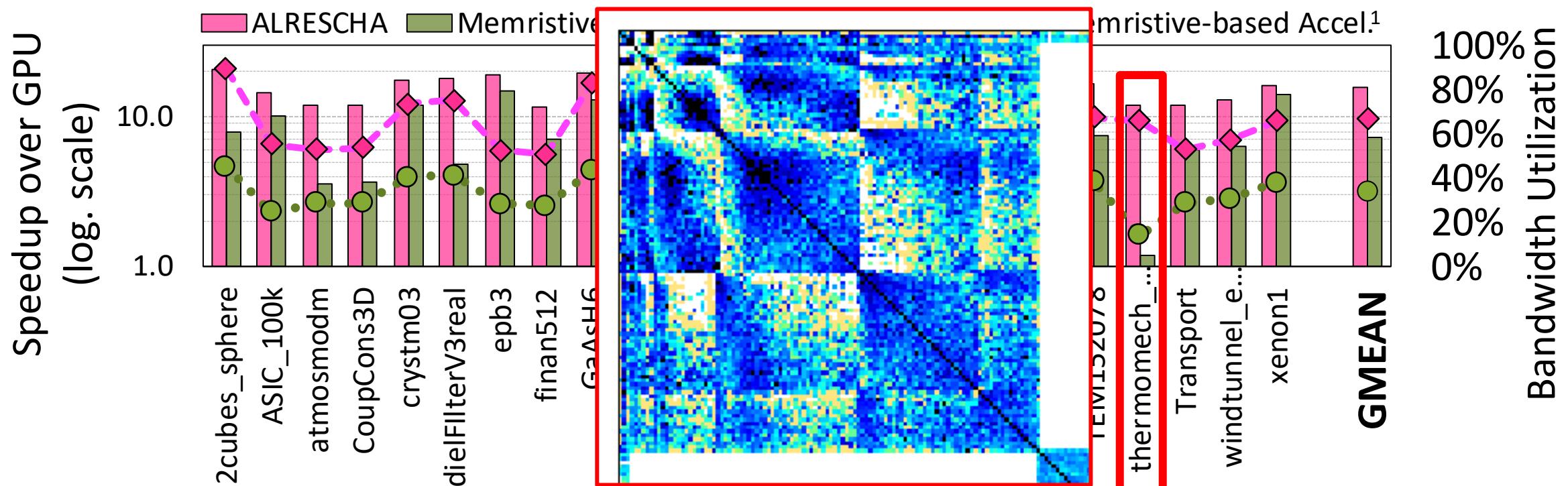


# Speedup for scientific workloads

74

Alrescha resolves performance bottleneck

- ▶ 2.1x speedup compared to emerging technologies
- ▶ 15.6x speedup over GPU



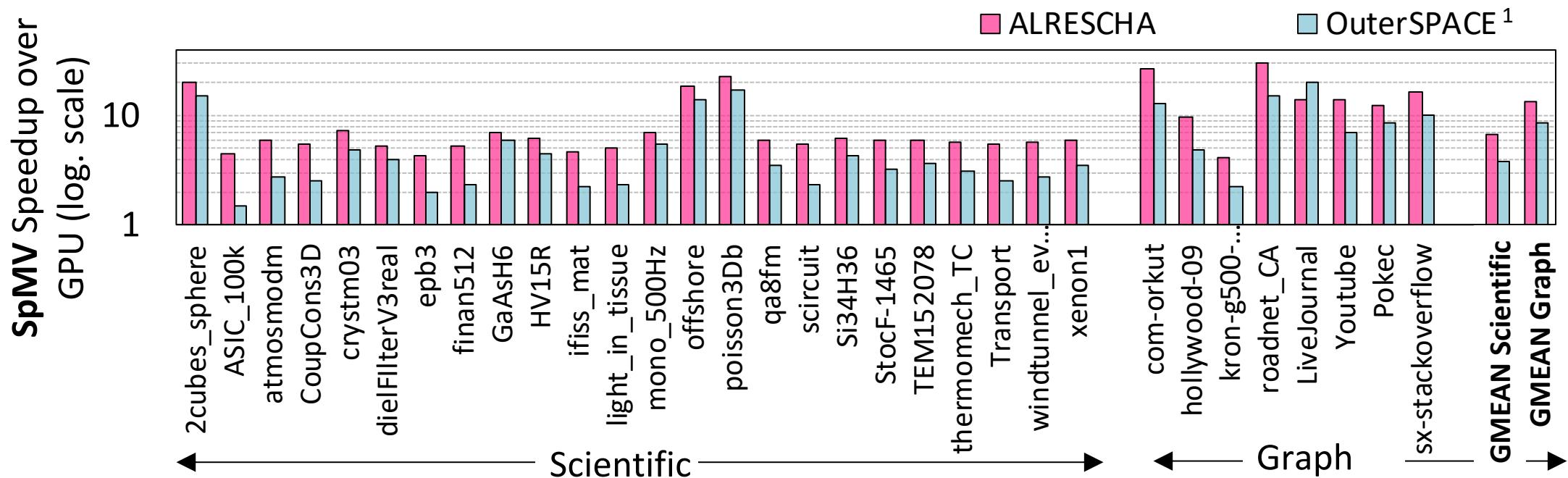
<sup>1</sup>B. Feinberg et al. "Enabling scientific computing on memristive accelerators," ISCA'18



# Speedup for Other Applications

Alrescha provides better reusability

- ▶ 13.6x speedup over GPU for scientific workloads
- ▶ 6.9x speedup over GPU for graph workloads



<sup>1</sup>S. Pal, J. Beaumont, et al. "Outerspace: An outer product based sparse matrix multiplication accelerator," HPCA'18



# Outline

76

- ▶ Using PDEs for modeling and key challenges
- ▶ Alrescha
  - ▶ Main contributions
  - ▶ Storage format
  - ▶ Reconfigurable microarchitecture
  - ▶ Broad applications
- ▶ Results
- ▶ **Conclusions**

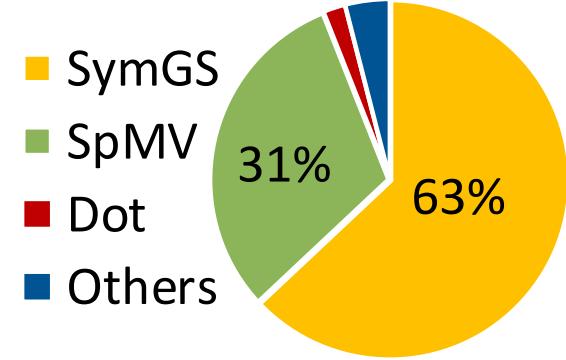


# Conclusions and Further Impacts

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Alrescha:

- ▶ Accelerates the **key kernels** of scientific problems
- ▶ Is the **first multi-kernel** sparse accelerator
- ▶ Has **broad applications** (e.g., scientific problems, graph, SpMV)
- ▶ Does not require emerging technologies



Further Impacts and Applications:

- ▶ Can accelerate any sparse problem that includes reduction operations
- ▶ Can leverage **partial reconfigurability** of FPGAs



# Backup Slides

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[Comparison with OuterSPACE](#)

[Mathematical expressions](#)

[Convert algorithm](#)

[Broad applications](#)

[Configuration table](#)

[Configuration and baselines](#)

[Sparse matrices](#)

[Reducing sequential operations](#)

[Graph results](#)

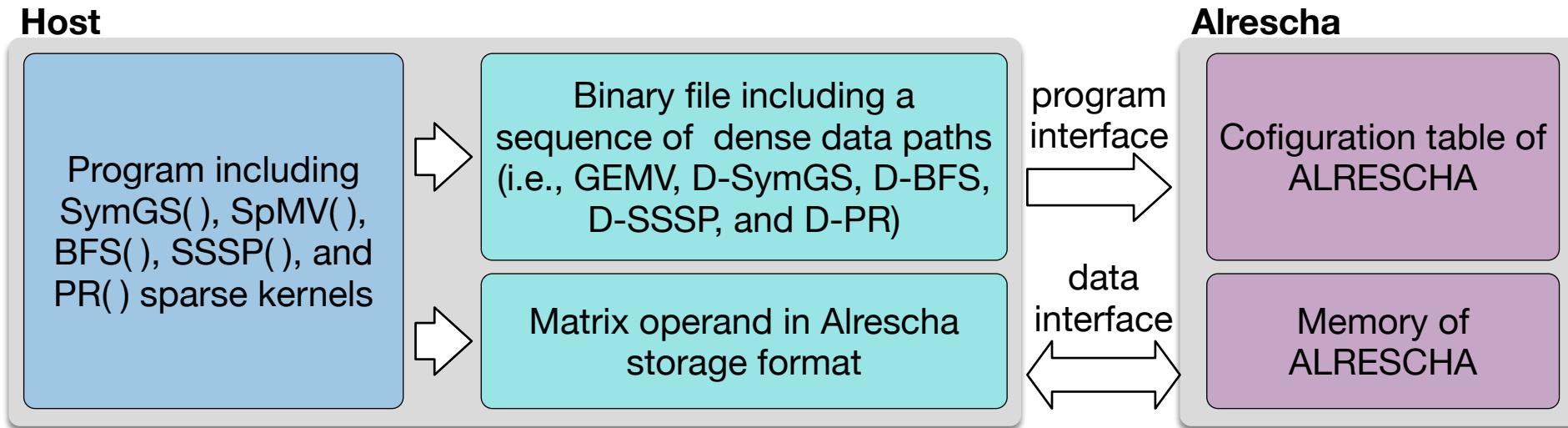
[Energy Consumption](#)

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# How does Alrescha work?

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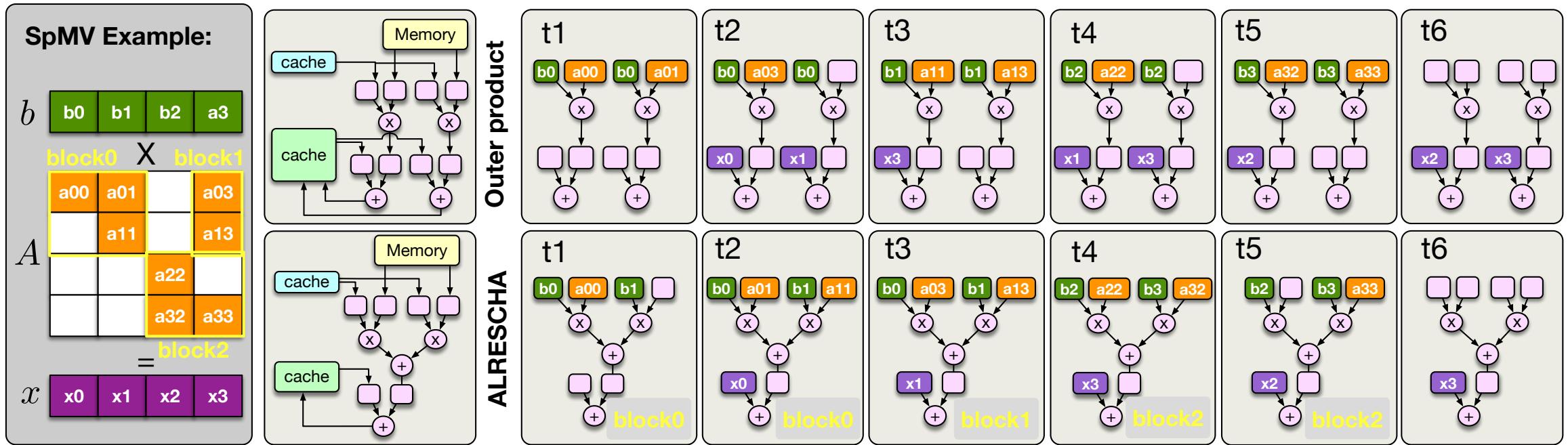


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# How Alrescha provides locality in output?

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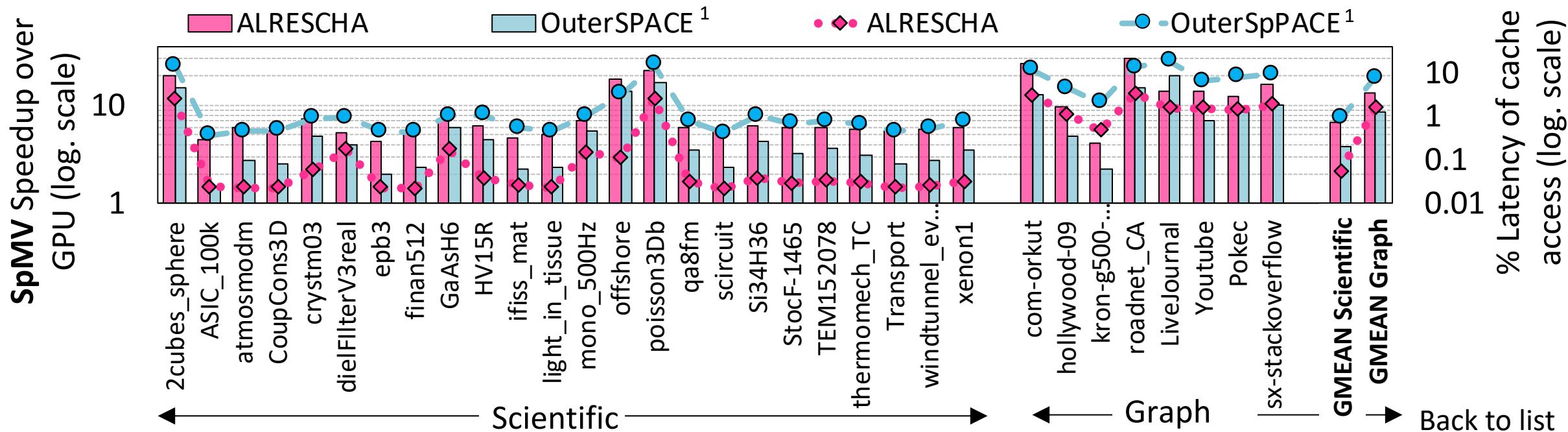


# Speedup for Other Applications

81

Alrescha provides better reusability

- ▶ 13.6x speedup over GPU for scientific workloads
- ▶ 6.9x speedup over GPU for graph workloads



<sup>1</sup>S. Pal, J. Beaumont, et al. "Outerspace: An outer product based sparse matrix multiplication accelerator," HPCA'18



# How do the exact mathematical expressions look like? 82

$$x_j^t = \frac{1}{A_{jj}^T} - (b_j - \sum_{i=1}^{j-1} A_{ij}^T \times x_i^t - \sum_{i=j+1}^n A_{ij}^T \times x_i^{t-1})$$



$$x_j^t = (\frac{1}{A_{jj}^T} - b_j) + (\sum_{i=1}^{j-1} A_{ij}^T \times x_i^t + \sum_{i=j+1}^n A_{ij}^T \times x_i^{t-1})$$

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# How do you program Alrescha?

## Algorithm 1 Convert Algorithm

```
1: function CONVERT(KernelType,  $A_{n \times n}$ ,  $\omega$ )
    $A_{n \times n}$ : sparse matrix,  $\omega$  : block width
   DP: Data path type
   l2r: left to right, r2l: right to left
2:    $Inx_{in} := 0, Inx_{out} := 0$ 
3:    $Blocks[] = \text{Split}(A, \omega)$  // partitions A to  $\omega \times \omega$  blocks
4:    $m = n/\omega$ 
5:   for ( $i = 1, i < m, i++$ ) do
6:     for ( $j = 1, j < m, j++$ ) do
7:       if ( $\text{nnz}(Blocks[i, j]) > 0$ ) then
8:         if KernelType != SymGS then
9:           DP = KernelType.DataPath
10:           $Inx_{in} = i.\omega, Inx_{out} = j.\omega$ 
11:          Order = l2r
12:          Op = port1 // the operand vector
13:        else
14:          if ( $i \neq j$ ) then
15:            DP = GEMV
16:             $Inx_{in} = j.\omega$ 
17:             $Inx_{out} = -1$  // no write to cache
18:            Order = l2r
19:            if ( $i > j$ ) then
20:              Op = port2 // which is  $x^{t-1}$ 
21:            else
22:              Op = port1 // which is  $x^t$ 
23:          else
24:            DP = D-SymGS
25:             $Inx_{in} = j.\omega, Inx_{out} = (i+1).\omega$ 
26:            Order = r2l
27:            Op = port2 // which is  $x^{t-1}$ 
28:   Add2Table(DP,  $Inx_{in}$ ,  $Inx_{out}$ , Order, Op)
```

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# Why Alrescha can execute other sparse problems?

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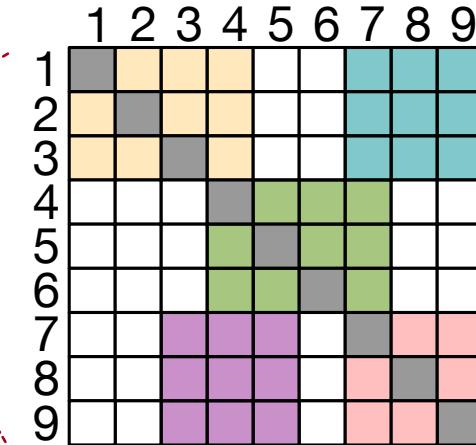
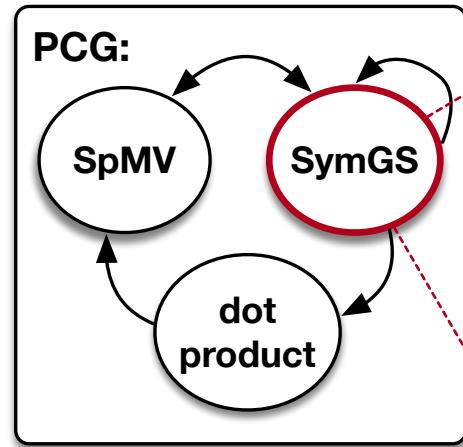
Sparse Kernel	Sparse Application	Dense Data Paths	Phase 1 (vector operation)				Phase 2 (reduce)	Phase 3 (assign)
			vector operand1	vector operand2	vector operand3	operation		
SymGS	PDE solving	D-SymGS/GEMV	a row of coefficient matrix	the vector from iteration (i-1)	the vector at iteration (i)	multiplication	sum	apply operation with $A^T$ and $b_j$ and update vector
SpMV	PDE solving and graph	GEMV	a row of coefficient matrix	the vector from iteration (i-1)	N/A	multiplication	sum	sum and update the vector
Page Rank	Graph	D-PR	a column of adjacency matrix	the out-degree vector of vertices	the rank vector at iteration (i-1)	AND/division	sum	rank vector update
BFS	Graph	D-BFS	a column of adjacency matrix	the frontier vector	N/A	sum	min	compare and update distance vector
SSSP	Graph	D-SSSP	a column of adjacency matrix	the frontier vector	N/A	sum	min	compare and update distance vector

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# What is configuration table?

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An arrow points from the matrix to a configuration table. The table lists five iterations (DP) with their corresponding parameters: Inx<sub>in</sub>, Inx<sub>out</sub>, Order, and Op.

DP	Inx <sub>in</sub>	Inx <sub>out</sub>	Order	Op
GEMV	7	-	l2r	$x^{t-1}$
D - SymGS	4	1	r2l	$x^{t-1}$
D - SymGS	7	4	r2l	$x^{t-1}$
GEMV	3	-	l2r	$x^t$
D - SymGS	9	7	r2l	$x^{t-1}$

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# What is the details of Alrescha & baseline config.

86

Floating point	double precision (64 bits)
Clock frequency	2.5 GHz
Cache	1KB, 64-Byte lines, 4-cycle access latency
RE latency	3 Cycles (sum: 3, min: 1)
ALU latency	3 Cycles
Memory	12 GB GDDR5, 288 GB/s

## GPU baseline

Graphics card	NVIDIA Tesla K40c, 2880 CUDA cores
Architecture	Kepler
Clock frequency	745MHz
Memory	12 GB GDDR5, 288 GB/s
Libraries	Gunrock [37] and CUSPARSE
Optimizations	row reordering (coloring) [8], ELL format

## CPU baseline

Processor	Intel Xeon E5-2630 v3 8-core
Clock frequency	2.4 GHz
Cache	64 KB L1, 256 KB L2, 20 MB L3
Memory	128 GB DDR4, 59 GB/s
Platforms	CuSha [39], GridGraph [38]

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# How do the scientific workloads look like?

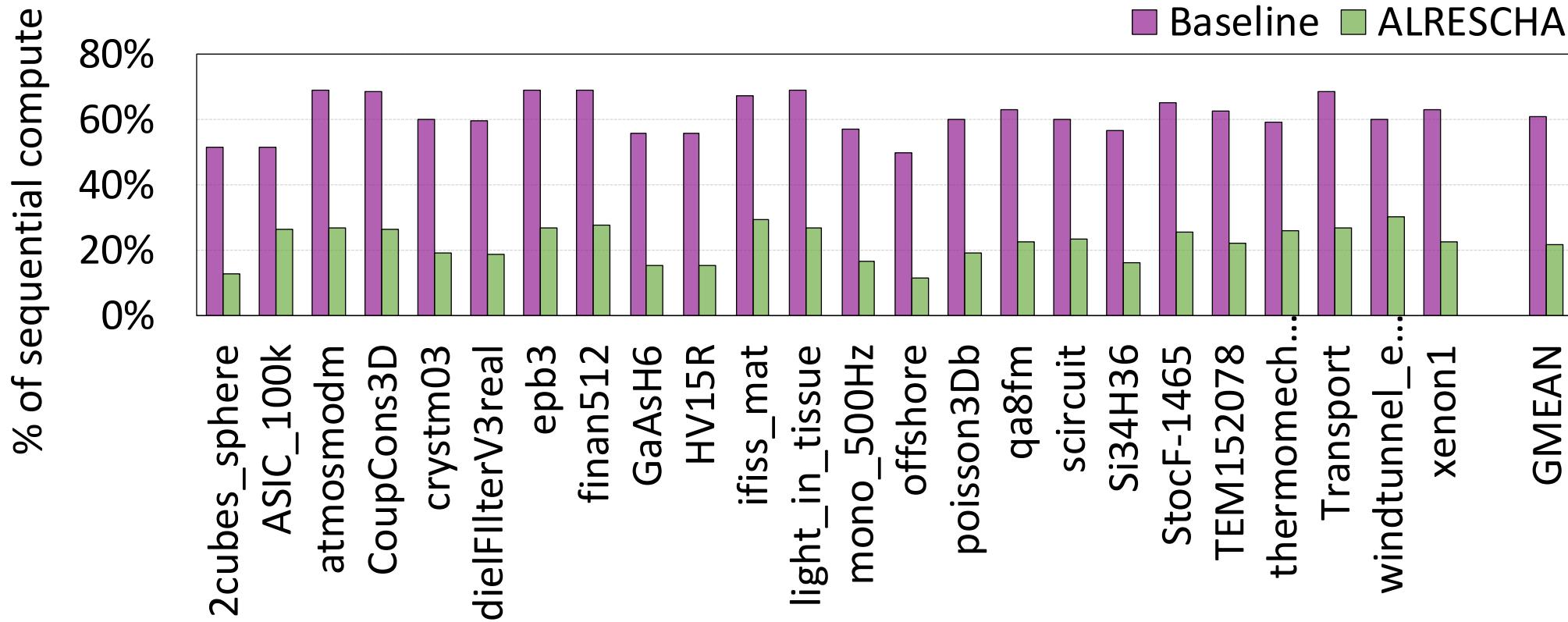
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Name	Row/Col	Kind	NNZ												
2cubes_sphere	101,492	Electromagnetic	1,647,264												
mono_500Hz	169,410	Acoustics Prob.	5,036,288												

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# How much Alrescha reduces sequential computations? 88

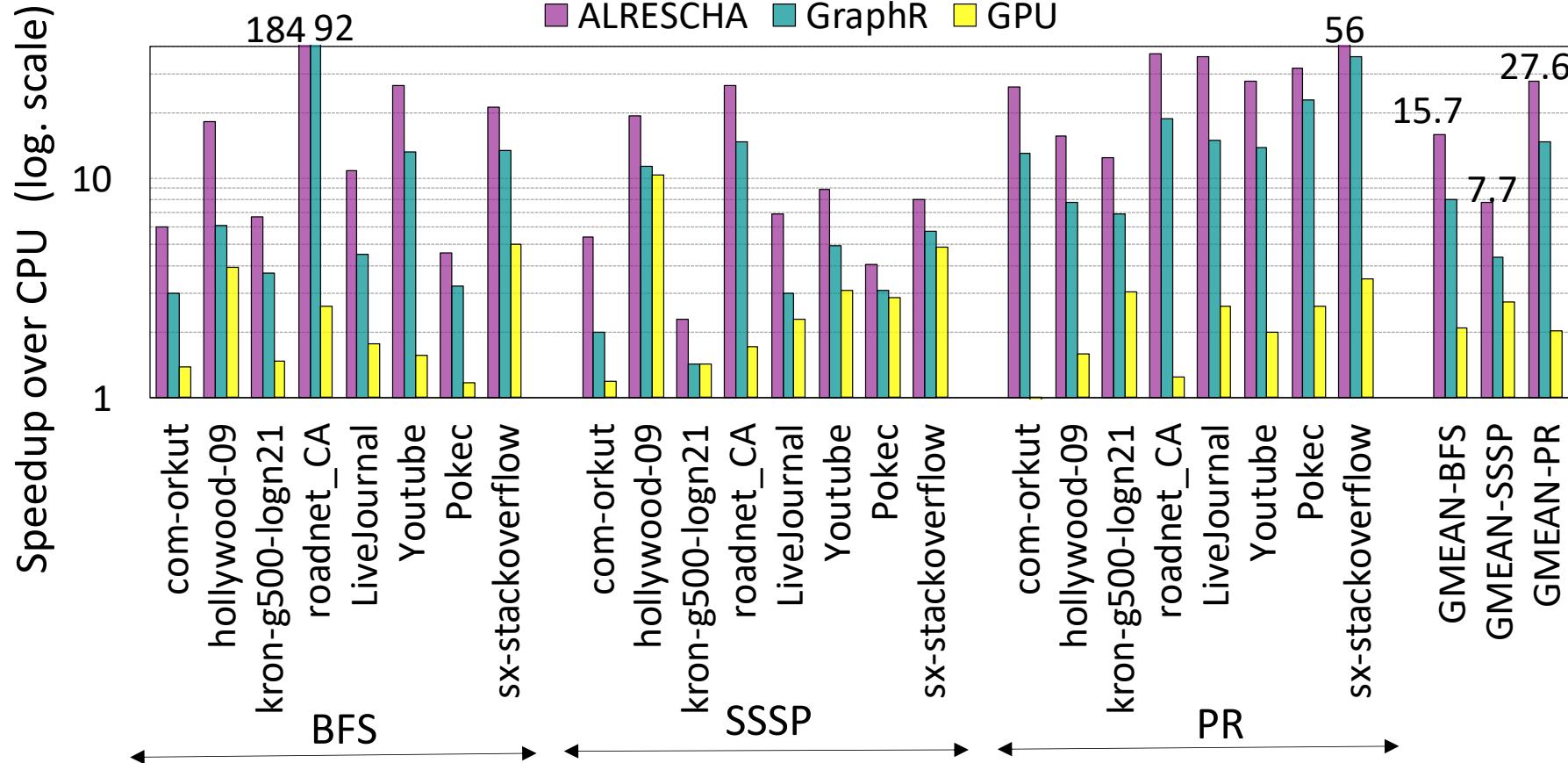


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# Can Alrescha accelerate graph algorithms?

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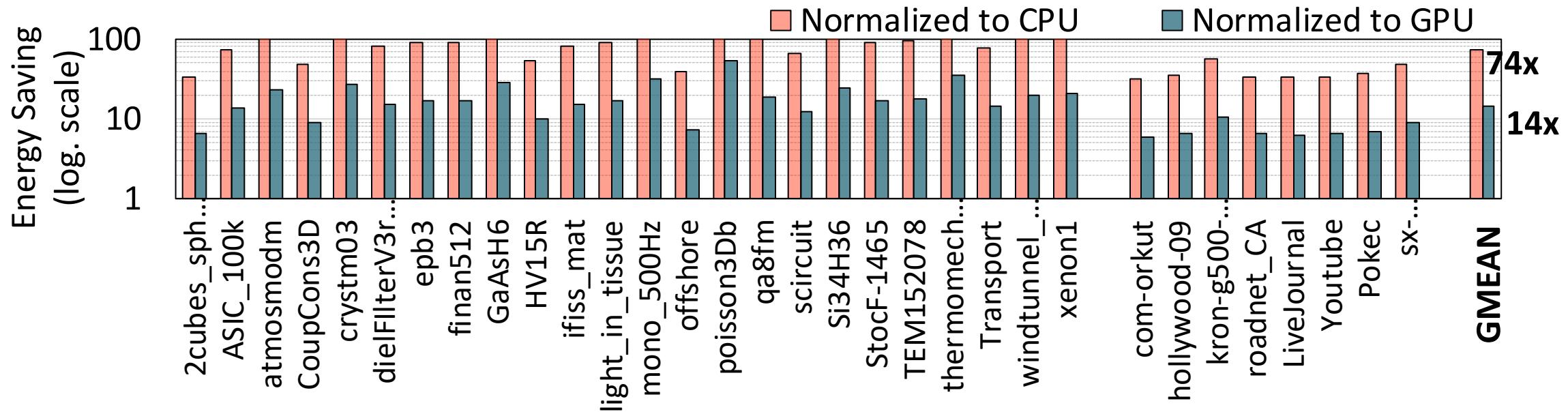


# Energy Consumption

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Alrescha substitutes many memory accesses with

- ▶ Computations
- ▶ Local cache accesses



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# Comparison with state-of-the-art accelerators

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	GraphR [24]	OuterSPACE [18]	Memristive-Based Accelerator [25]	Row Reordering Matrix Coloring [8]	Alrescha (our work)
Application Domain	Graph	Graph (only SpMV)	PDE solver	PDE solver	Graph and PDE solver
Hardware	Multi-Kernel Support	✗	✗	✗	✓
	BW Utilization	Low	Moderate	Low	High
	NOT Transferring Meta-data	✗	✗	✗	✓
	Processing Type	ReRAM Crossbar	PEs connected in a high-speed crossbar	heterogeneous Memristive crossbar	Fixed vector processor and a small reconfigurable switch
	Cache Optimizations For Frequently-Used Vectors	N/A	✗	N/A	✓
	Reconfigurability	✗	Only for cache hierarchy	✗	✓
Techniques	Storage Format	4×4 COO	CSR	multi-size blocks (64×64, 128×128, 256×256, 512×512)	ELL 8×8 blocking with fine-grained in-block ordering
	Resolving Limited Parallelism	N/A	N/A	✗	✓ (Instruction-level, limited by sparsity pattern)

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