CMSC 311- Computer Organization

Fall 1995 - Assignment #3 (solution)

1)

A	B	E	x	A	B	Ja	Ka	Jb	Kb
0	0	0	0	0	0	0	x	0	x
0	0	0	1	0	0	0	x	0	x
0	0	1	0	1	1	1	x	1	x
0	0	1	1	0	1	0	x	0	x
0	1	0	0	0	1	0	x	x	0
0	1	0	1	0	1	0	x	x	0
0	1	1	0	0	0	0	x	x	1
0	1	1	1	1	0	1	x	x	1
1	0	0	0	1	0	x	0	0	x
1	0	0	1	1	0	x	0	0	x
1	0	1	0	0	1	x	1	1	x
1	0	1	1	1	1	z	0	1	x
1	1	0	0	1	1	x	0	x	0
1	1	0	1	1	1	x	0	x	0
1	1	1	0	1	0	x	0	x	1
1	1	1	1	0	0	x	1	x	1

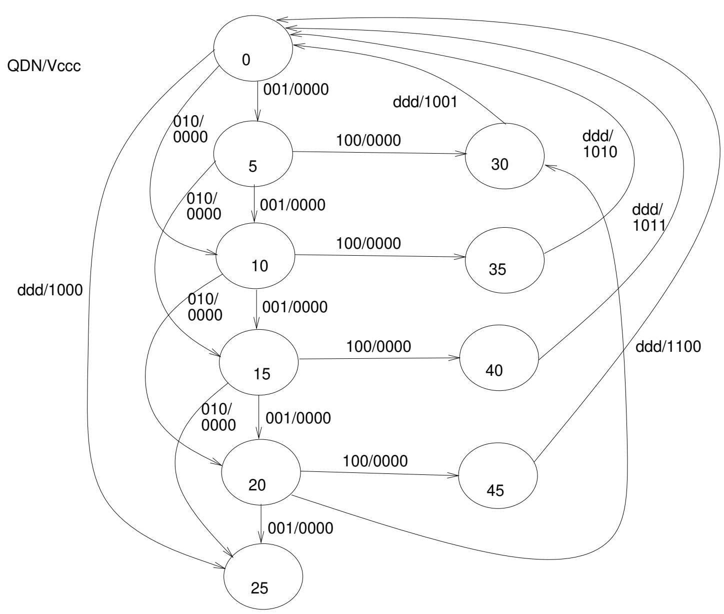
Ja = (Bx + B'x') E

Ka = (Bx + B'x') E

Jb = E

Kb = E

2) State diagram



State Table

Inputs (NDQ)

Present	**000**	**001**	**010**	**100**	**Vend**	**Change 210**
0000	0	1	2	5	0	000
0001	1	2	3	6	0	000
0010	2	3	4	7	0	000
0011	3	4	5	8	0	000
0100	4	5	6	9	0	000
0101	0	NP	NP	NP	1	000
0110	0	NP	NP	NP	1	001
0111	0	NP	NP	NP	1	010
1000	0	NP	NP	NP	1	011
1001	0	NP	NP	NP	1	100

3)

a) Inverters - 2pins each 12/2 = 6 gates 7404

b) 2 input XOR - 3 pins each 12/3 = 4 gates 7486

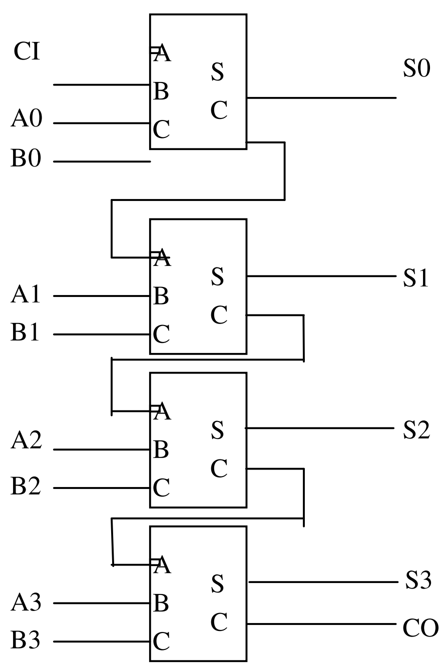
c) 3 input OR - 4 pins each 12/4 = 3 gates

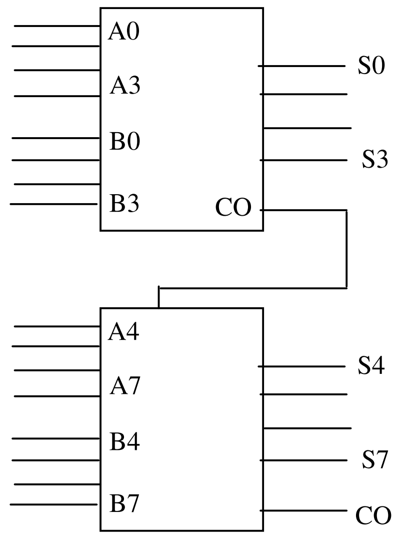
d) 5 input AND - 5 pins each 12/5 = 2 gates 7421

e) 8 input NAND - 9 pins 12/9 = 1 gate 74107

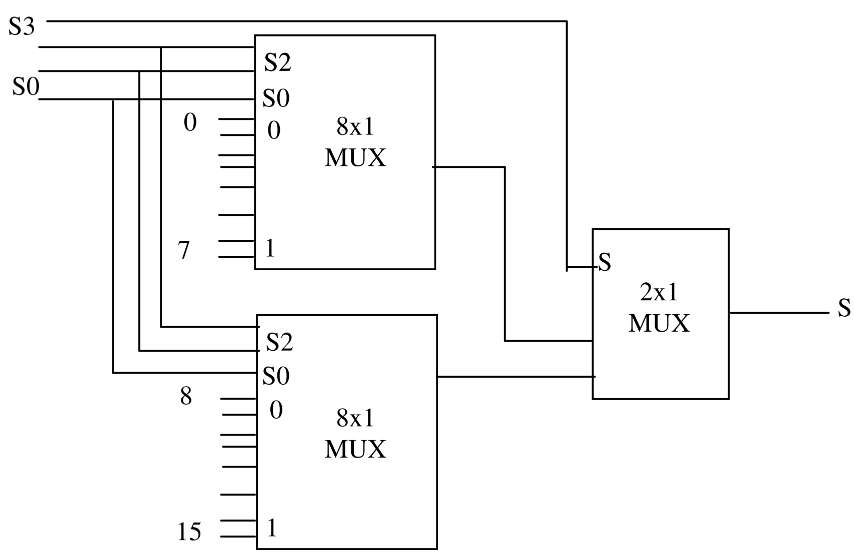
4)

a) Design a 4 bit adder using 4 full adders.




A0
A3
B0
B3
CO
S0
S3
A4
A7
B4
B7
S4
S7
CO

5)


S3
S0
S2
S0
0
0
8x1
MUX
7
1
S
2x1
MUX
S
S2
S0
8
0
8x1
MUX
15
1