CMSC 311
Solutions to Homework 7

Problem 1. A and B are input to the select lines. The two outputs from lines 01 and 10 are input into the OR gate.

Problem 2. We will have four copies of the following side-by-side: A 4×1 multiplexer whose output goes into a D flip-flop. The four data lines input to the multiplexer are

Input 00: 0.

Input 01: A line from outside the circuit.

Input 10: The output of the D flip-flop immediately to its right.

Input 11: The output of the D flip-flop immediately to its left.

The left endpoint has 0 input for line 11, and the right endpoint has 0 input for line 10,

Problem 3. Same as above except the output of the multiplexer is not connected directly into the T flip-flop. The output of the multiplex and of the T flip-flop go through an XOR gate, which is then fed into the T flip-flop.

Problem 4. Assume you have logic that allows three values (trits) 0, 1, or 2. Assume all gates in this logic have two inputs.

(a) SUM

	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

CARRY

	0	1	2
0	0	0	0
1	0	0	1
2	0	1	1

standard OR gate (on inputs 0 and 1)

(b) Connect inputs A and B both to a SUM gate and to a CARRY gate.

(c) Connect A and B to a SUM gate and connect the output of that and CARRY_{IN} to another SUM gate to get the final SUM.

Connect A and B to a CARRY gate. Connect the output of the A and B SUM gate and C to a CARRY gate. OR these two carry values to get the $\text{CARRY}_{\text{OUT}}$