#### **Addressing modes**

MIPS has 5 ways of addressing data (see fig. 3.17)

- 1. immediate: data is in instruction itself
- 2. register: register number in instruction tells which register contains data
- 3. base/offset: offset value added to base register
- 4. PC-relative: offset added to PC
- 5. pseudodirect: offset from instruction merged with PC

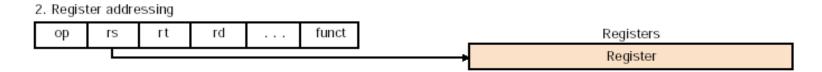
# Addressing modes: immediate

1. Immediate addressing

op rs rt Immediate

data is in instruction itself: I-type instruction how many bits? signed or unsigned?

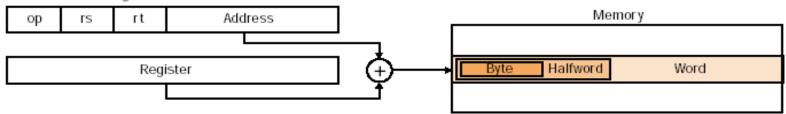
## Addressing modes: register



register number in instruction tells which register contains data register may contain data (add) or address (jr) R-type instructions

#### Addressing modes: base/offset

3. Base addressing



Addr <-- R[s] + (IR<sub>15</sub>)<sup>16</sup>::IR<sub>15-0</sub>

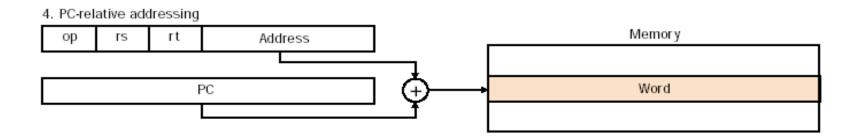
16-bit offset (immed) value in instruction is added to address value in register

sign-extend offset

result is address in memory which contains data

data may be byte, halfword, word depending on instruction used in load and store instructions (I-type)

### Addressing modes: PC-relative

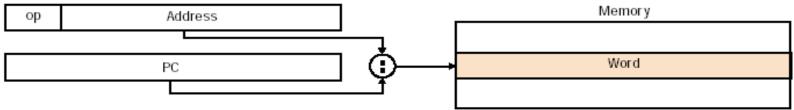


$$PC = PC + (IR_{15})^{14} :: IR_{15-0} :: 00$$

similar to base addressing, but offset is added to value of PC extra 00 concatenated to end of offset used for branch instructions (I-type)

### Addressing modes: pseudo-direct





 $PC \iff PC_{31-28} :: IR_{25-0} :: 00$ 

direct addressing: complete 32-bit address

26 bits in instruction are concatenated with PC

4 high-order PC bits

00 for low-order bits

can access 1/16 of all possible MIPS addresses

note that figure is not clear on which bits are actually used from PC

J-type instructions

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