Register allocation

Motivation

- registers much faster than memory
- limited number of physical registers
- keep values in registers as long as possible (minimize number of load/stores executed)

Register allocation

1. for simplicity, assume an infinite set of virtual registers during optimization & code gen.
2. map virtual registers onto finite # of registers
3. assign virtual registers to physical registers

Approaches

- local allocation
  - top-down — assign registers by frequency
  - bottom-up — spill registers by reuse distance
- global allocation
  - top-down — color interference graph
  - bottom-up — split live ranges
Local register allocation

Top-down

• rank virtual registers by # uses in block
• reserve sufficient registers for memory operations
• assign remaining physical registers by rank
• problem – assignment fixed for entire block

Bottom-up

• put physical registers on free list
• for each instruction in order
  – if operand not in register, assign free register
  – if free list empty, reclaim register holding value whose use is furthest in future

Example

<table>
<thead>
<tr>
<th></th>
<th>Top-down</th>
<th>Bottom-up</th>
</tr>
</thead>
<tbody>
<tr>
<td>1) a = b + c</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2) c = a + d</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3) a = a + c</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Global register allocation (top-down)

Register coloring

- map register allocation to graph coloring
- major steps
  1. global data-flow analysis to find live ranges
  2. build and color interference graph
  3. if unable to color, spill registers and repeat

Live ranges

- all definitions which reach a use, plus all uses reached by these definitions

\[
\begin{align*}
a &= \\
b &= \\
&= a \\
&= b \\
&= b
\end{align*}
\]

- a single virtual register name may comprise several live ranges

\[
\begin{align*}
a &= \\
&= a \\
a &= \\
&= a
\end{align*}
\]
Interference

Using live ranges, an *interference graph* is constructed where

- vertices represent live ranges
- edges represent *interferences* between two live ranges, *i.e.*, both ranges are live at some point and cannot occupy the same register
- a coloring represents a register assignment
  (one color per register)

Note that the abstraction subtly changes our goals. However, the separation of optimization and allocation justifies the goal of minimal coloring.

Building the interference graph

- at each point $p$ in the program, add edge $(x, y)$ for all pairs of live ranges $x, y$ live at $p$

Example

\[
\begin{align*}
a &= a \\
  &= a \\
b &= a \\
  &= b
\end{align*}
\]
Coloring

Graph coloring

- given graph, find assignment of colors to each node such that no neighbors have same color
- determining whether a graph may be colored with $k$ colors is NP-hard for $k \geq 2$

Register coloring

- find a legal coloring given $k$ colors,
- $k$ is the number of available registers

Chaitin’s et al.’s algorithm [1981]

1. Repeatedly remove nodes with degree $< k$ from the graph and push them on a stack.

2. If every remaining node is degree $\geq k$, spill node with lowest spill cost and remove it from the graph.

3. Reassemble the graph with nodes popped from the stack. As each node is added to the graph, choose a color differing from neighbors in the graph.
Simplification Example
Optimistic coloring

What if we have two registers? Chaitin et al.'s algorithm would spill a variable

Brigg's et al.'s algorithm [1989]

1. Repeatedly remove nodes with degree $< k$ from the graph and push them on a stack.
2. If every remaining node is degree $\geq k$, select node with lowest spill cost and remove it from the graph.
3. Reassemble the graph with nodes popped from the stack. If node cannot be colored, spill it.

Deferring spill decisions helps when

- neighbors of a node are the same color
- a neighboring node has already been spilled
Spilling

Spill code

- when too few registers, *spill* register to memory
- insert load (before use) and store (after def)

\[
\begin{align*}
  a &= \quad r1 &= \quad r1 = \\
  b &= \quad r2 &= \quad \text{store } r1, \ a \\
  &= b &= r2 &= r1 = \quad \text{load } r1, \ a \\
  &= a &= r1 &= r1
\end{align*}
\]

Effects

- breaks live range into many small live ranges
- reduces chance of interference
- very expensive, introduces load/store for each use/def over entire live range

Reducing spill code

- value modified – store register to memory (dirty)
- read-only value – reload from memory (clean)
- constant value – recompute value (rematerialize)
Estimating Spill Costs

Which live ranges to spill? Two goals

- try to minimize cost of spill
- try to maximize decrease in interference
  (reduce need for more spills)

Cost functions

<table>
<thead>
<tr>
<th>$degree(v)$</th>
<th># of edges for $v$ in interference graph</th>
</tr>
</thead>
<tbody>
<tr>
<td>$depth(I)$</td>
<td>loop nesting depth of instruction I</td>
</tr>
<tr>
<td>$cost(v)$</td>
<td>$\sum_{v \text{ live at instr I}} 10^{depth(I)}$</td>
</tr>
</tbody>
</table>

Cost estimate heuristics

$h_0: \frac{cost(v)}{degree(v)}$ [Chaitin et al.]

$h_1: \frac{cost(v)}{degree(v)^2}$

Approach

- apply different spilling heuristics, pick best result
- most expense is in building interference graph
- spill cost estimates can be calculated efficiently
Global register allocation (bottom-up)

Live range splitting

- insert copies to split up live ranges
- hope to reduce spilling
- also controls spill code placement

\[
\begin{align*}
a &= a = a \\
&= a &= a
\end{align*}
\]

Coalescing (Subsumption)

- allocate source and destination of copy to same register to eliminate register-to-register copies
- combines live ranges
- can clean up unnecessary splits

\[
\begin{align*}
a &= r1 = \\
b &= a \\
&= b &= r1
\end{align*}
\]
Live range splitting

One approach

1. locally allocate registers for each basic block
2. prioritize live ranges by estimated spill cost
3. allocate registers to live ranges
4. split live range if no colors available

# Enhancement examples

<table>
<thead>
<tr>
<th>Original</th>
<th>Chaitin</th>
<th>Splitting</th>
<th>Rematerialized</th>
</tr>
</thead>
<tbody>
<tr>
<td>( p \leftarrow f() )</td>
<td>( p \leftarrow f() )</td>
<td>( p \leftarrow f() )</td>
<td>( p \leftarrow f() )</td>
</tr>
<tr>
<td></td>
<td>( \text{spill } p )</td>
<td>( \text{spill } p )</td>
<td></td>
</tr>
<tr>
<td>( y \leftarrow y + [p] )</td>
<td>( \text{reload } p )</td>
<td>( \text{reload } p )</td>
<td>( p \leftarrow f() )</td>
</tr>
<tr>
<td>( \text{...regs...} )</td>
<td>( \text{...regs...} )</td>
<td>( \text{...regs...} )</td>
<td>( \text{...regs...} )</td>
</tr>
<tr>
<td>( p \leftarrow p + 1 )</td>
<td>( \text{reload } p )</td>
<td>( p \leftarrow p + 1 )</td>
<td>( p \leftarrow p + 1 )</td>
</tr>
<tr>
<td></td>
<td>( \text{spill } p )</td>
<td>( p \leftarrow p + 1 )</td>
<td>( p \leftarrow p + 1 )</td>
</tr>
</tbody>
</table>
Combining Scheduling and Allocation

Allocation before scheduling

- register assignment introduces dependences
- reduces freedom of scheduler
- example

\[
\begin{align*}
\text{load } vr1,a & \quad \text{load } r1,a & \quad \text{load } r1,a \\
vr3 = vr1 & \quad r3 = r1 & \quad \text{load } r2,b \\
\text{load } vr2,b & \quad \text{load } r1,b & \quad r3 = r1 \\
vr4 = vr2 & \quad r4 = r1 & \quad r4 = r2
\end{align*}
\]

Scheduling before allocation

- lengthens live range of virtual registers
- increases register pressure, causes spills
- need to schedule spill code after allocation
- example

\[
\begin{align*}
\text{load } vr1,a & \quad \text{load } vr1,a \\
vr4 = vr1 & \quad \text{load } vr2,b \\
\text{load } vr2,b & \quad \text{load } vr3,c \\
vr5 = vr2 & \quad vr4=vr1 \\
\text{load } vr3,c & \quad vr5=vr2 \\
vr6 = vr3 & \quad vr6=vr3
\end{align*}
\]
Combining Scheduling and Allocation

We see that instruction scheduling and register allocation are interdependent

What can we do?

Assigning registers

- first-fit — lowest number available register (reduces total number of registers assigned)
- round-robin — cycle through all registers (reduces memory-related dependences)

Change ordering

- postpass — allocate then schedule
- prepass — schedule then allocate
- multipass — schedule, allocate, then schedule

Integrated prepass scheduling

- schedule instructions first as prepass
- bias schedule to reduce local register pressure
- allocate registers after scheduling