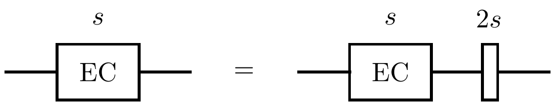
Solution Set #8

Quantum Error Correction
Instructor: Daniel Gottesman

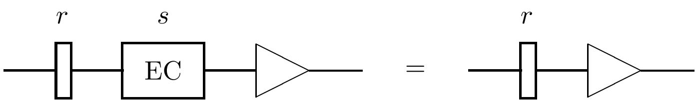
Problem #1. Fault-Tolerance With SWAPs Within a Code Block

a) Basically, we want each fault during the gadget to count as two errors. Thus, EC property 1 becomes



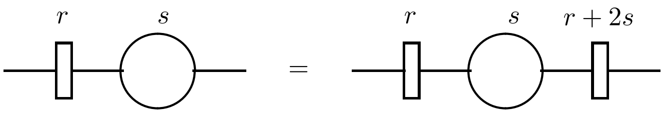
$(2s \leq t)$

and EC property 2 becomes



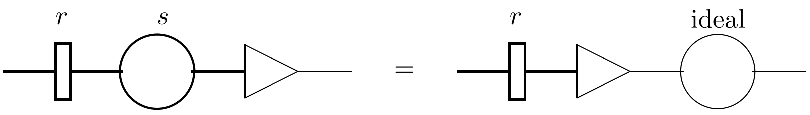
$(r + 2s \leq t)$

Similarly, we get a new gate property 1



$(r + 2s \leq t)$

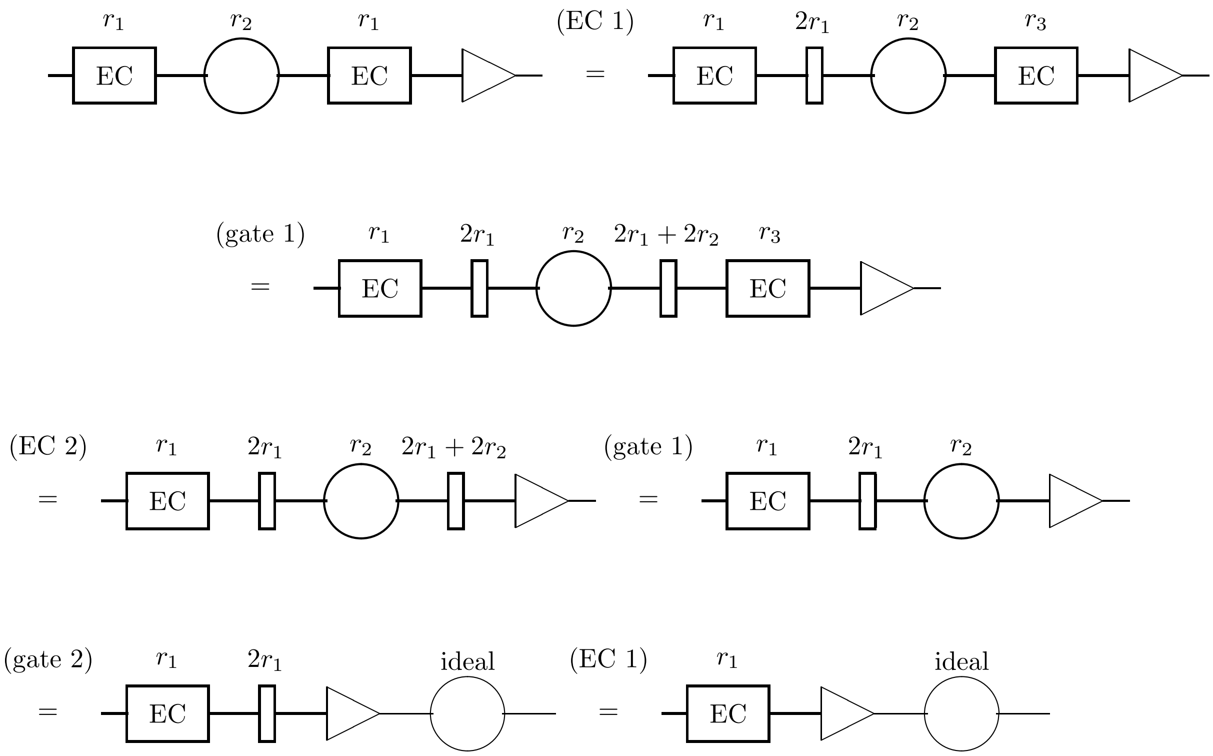
and gate property 2



$(r + 2s \leq t)$

Our old gadgets, modified to use nearest-neighbor gates everywhere, with SWAP gates to move qubits around, do not satisfy the old definition of fault tolerance, since a single failed SWAP gate can cause two errors, but do satisfy these revised properties.

b) We have much the same proof as before. Now, we allow r_1 faults in the first EC step, r_2 faults in the gate gadget, and r_3 faults in the second EC step, but $r_1 + r_2 + r_3 \leq 1$ even though $t = 2$. Thus, $2(r_1 + r_2 + r_3) \leq t$.



c) Again a single fault can cause two errors in neighboring locations, just as with SWAP gates. That is, each fault can accomplish something that could only be done with two faults in the original model from the lectures. Our FT gadgets therefore no longer satisfy the old conditions, but do still satisfy the conditions from part a, since they result from replacing each fault during a gadget with two faults.

Now let us consider the behavior of a SWAP gate under level reduction. A FT SWAP gate consists of a number of physical SWAP gates, and (depending how exactly we implement it), two failed physical SWAP gates (or one failed SWAP gate and one other fault during one of the EC steps in the SWAP extended rectangle) can cause a logical SWAP gate to fail. Thus, after level reduction, the error rate for a physical SWAP gate decreases to $O(p^2)$, just like any other gate.

However, note that this only is malignant (in the sense of causing correctness to fail) if one of the faulty SWAPs is between physical qubits in the same block of the code. This is because SWAP does not propagate errors, and we are using a code with $t = 2$, meaning we need 3 errors per block to cause a logical error. Thus, if there are only two faults, we should (in an optimal analysis) replace a bad SWAP extended rectangle with two faults by a SWAP gate which only causes an error on one of the two qubits involved. In order for both qubits to have errors after level reduction, we need a SWAP extended rectangle with three faults. That is, under level reduction, we get a SWAP gate with two very different kinds of errors. We get errors on only a single qubit involved in the SWAP gate at a rate $O(p^2)$, and we have errors on both of the two qubits involved in the SWAP gate at $O(p^3)$. This is in contrast to a CNOT gate or other two-qubit gate, which propagate errors from block to block, and for which level reduction can therefore leave errors on both qubits involved in the gate with probability $O(p^2)$.

Correlated two-qubit errors experience a similar effect. Two faults, one of which is a correlated two-qubit fault within a block, can cause an error on a single block of the code. To get simultaneous errors on two adjacent blocks, we need three physical faults: a two-qubit fault in each block, plus another two-qubit fault causing one physical error in each block. (Another possibility is three two-qubit faults, each of which introduces one error per block.) Since the two-qubit errors are only on adjacent qubits, this arrangement can only happen when the two blocks are physically adjacent. One difference from the SWAP gate case is in the constant factors: since the SWAP gate involves moving all the qubits of one block past all the qubits of the other block, there are many more opportunities for a faulty SWAP gate interacting qubits from both blocks, whereas in the case of correlated two-qubit errors, only at the border of the two blocks is there a possibility of having a single two-qubit fault cause one physical error per block.

The upshot is that when there is a source of correlated two-qubit errors at error rate p, the probability of a correlated two-qubit error between adjacent qubits after level reduction is only $O(p^3)$. There are also one-qubit errors occurring after level reduction with probability $O(p^2)$, and the physical two-qubit errors contribute to that. This is similar to the situation with SWAP gates, which are bad with probability $O(p^2)$, but only have errors on both qubits with probability $O(p^3)$. If we want to define a good error model for concatenated SWAP gates, we should separate out these two types of SWAP gate errors, which requires adding an additional type of error to our original model (bad SWAP gates with error on only one qubit), whereas our model of correlated two-qubit errors was already in addition to a direct source of single-qubit storage errors.

Problem #2. Pseudothresholds for Fault-Tolerance

a) The largest single-bit operation is the NOT gate (performed transversally), and the NOT extended rectangles contains 3 NOT gates plus two EC steps, for a total of 39 single-bit operations, 24 CNOTs, and 6 Toffoli gates, so

$$\begin{aligned} p_1(\text{single}) =& \binom{39}{2} p_0(\text{single})^2 + 39 \cdot 24 p_0(\text{single}) p_0(\text{CNOT}) + \binom{24}{2} p_0(\text{CNOT})^2 && (1)\\ &+ 39 \cdot 6 p_0(\text{single}) p_0(\text{Tof}) + 24 \cdot 6 p_0(\text{CNOT}) p_0(\text{Tof}) + \binom{6}{2} p_0(\text{Tof})^2 && (2)\\ =& 741 p_0(\text{single})^2 + 936 p_0(\text{single}) p_0(\text{CNOT}) + 276 p_0(\text{CNOT})^2 && (3)\\ &+ 234 p_0(\text{single}) p_0(\text{Tof}) + 144 p_0(\text{CNOT}) p_0(\text{Tof}) + 15 p_0(\text{Tof})^2. && (4) \end{aligned}$$

The CNOT rectangle has 3 CNOTs and 4 EC steps, for a total of 72 single-bit operations, 51 CNOTs, and 12 Toffoli gates, giving

$$\begin{aligned} p_1(\text{CNOT}) =& \binom{72}{2} p_0(\text{single})^2 + 72 \cdot 51 p_0(\text{single}) p_0(\text{CNOT}) + \binom{51}{2} p_0(\text{CNOT})^2 && (5)\\ &+ 72 \cdot 12 p_0(\text{single}) p_0(\text{Tof}) + 51 \cdot 12 p_0(\text{CNOT}) p_0(\text{Tof}) + \binom{12}{2} p_0(\text{Tof})^2 && (6)\\ =& 2556 p_0(\text{single})^2 + 3672 p_0(\text{single}) p_0(\text{CNOT}) + 1275 p_0(\text{CNOT})^2 && (7)\\ &+ 864 p_0(\text{single}) p_0(\text{Tof}) + 612 p_0(\text{CNOT}) p_0(\text{Tof}) + 66 p_0(\text{Tof})^2. && (8) \end{aligned}$$

The Toffoli rectangle has 3 Toffolis and 6 EC steps, for a total of 108 single-bit operations, 72 CNOTs, and 21 Toffoli gates, giving us

$$\begin{aligned} p_1(\text{Tof}) =& \binom{108}{2} p_0(\text{single})^2 + 108 \cdot 72 p_0(\text{single}) p_0(\text{CNOT}) + \binom{72}{2} p_0(\text{CNOT})^2 && (9)\\ &+ 108 \cdot 21 p_0(\text{single}) p_0(\text{Tof}) + 72 \cdot 21 p_0(\text{CNOT}) p_0(\text{Tof}) + \binom{21}{2} p_0(\text{Tof})^2 && (10)\\ =& 5778 p_0(\text{single})^2 + 7776 p_0(\text{single}) p_0(\text{CNOT}) + 2556 p_0(\text{CNOT})^2 && (11)\\ &+ 2268 p_0(\text{single}) p_0(\text{Tof}) + 1512 p_0(\text{CNOT}) p_0(\text{Tof}) + 210 p_0(\text{Tof})^2. && (12) \end{aligned}$$

b) Under this assumption, the recursion relations from part a simplify to

$$p_1(\text{single}) = 5418p^2 \tag{13}$$
$$p_1(\text{CNOT}) = 21858p^2 \tag{14}$$
$$p_1(\text{Tof}) = 49320p^2. \tag{15}$$

We then find $p_1(\text{single}) \leq p_0(\text{single}) = p$ when $p = 1/5418$, $p_1(\text{CNOT}) \leq p_0(\text{CNOT}) = 2p$ when $p = 1/10929$, and $p_1(\text{Tof}) \leq p_0(\text{Tof}) = 3p$ when $p = 1/16440$. That is, we find

$$p_T(1,\text{single}) = 1/5418 \approx 1.85 \times 10^{-4} \tag{16}$$
$$p_T(1,\text{CNOT}) = 2/10929 \approx 1.83 \times 10^{-4} \tag{17}$$
$$p_T(1,\text{Tof}) = 3/16440 \approx 1.82 \times 10^{-4}. \tag{18}$$

c) The equations from part a can be used for each additional level of concatenation to give the formulas that determine $p_j(\text{single})$, $p_j(\text{CNOT})$, and $p_j(\text{Tof})$ from the values at level $j-1$. In particular, under the given set of assumptions, we find that

$$p_2(\text{single}) \approx 5.19 \times 10^{11} p^4 \tag{19}$$
$$p_2(\text{CNOT}) \approx 2.17 \times 10^{12} p^4 \tag{20}$$
$$p_2(\text{Tof}) \approx 5.06 \times 10^{12} p^4 \tag{21}$$

We then find pseudothresholds

$$p_T(2,\text{single}) \approx 1/(5.19 \times 10^{11})^{1/3} \approx 1.2 \times 10^{-4} \tag{22}$$
$$p_T(2,\text{CNOT}) \approx 2(2/2.17 \times 10^{12})^{1/3} \approx 2.0 \times 10^{-4} \tag{23}$$
$$p_T(2,\text{Tof}) \approx 3(3/5.06 \times 10^{12})^{1/3} \approx 2.5 \times 10^{-4} \tag{24}$$

It is worth noting that while the single-bit operations have the lowest pseudothresholds, that pseudothreshold corresponds to the largest value of p, while the Toffoli gate pseudothreshold corresponds to the smallest value of p.

d) For any given starting point $(p_0(\text{single}), p_0(\text{CNOT}), p_0(\text{Tof}))$ on or off the $1:2:3$ ray, we could iterate the map from part a many times. If at any level, all three error rates decrease when another level of concatenation is added, then we know they will continue to decrease, indicating that the starting point was inside the threshold surface. That will therefore be our criterion here.

For both parts b and c, the most restrictive pseudothreshold is for the Toffoli gate, in the sense that it corresponds to the lowest value of p, so when we are below the Toffoli gate pseudothreshold (along the $1:2:3$ ray), we are certainly below the threshold surface. From part b, we find that we are below the threshold surface if $p \leq 6.0 \times 10^{-5}$, whereas from part c, we find that we are below the threshold surface if $p \leq 8.4 \times 10^{-5}$. Both are lower bounds, but the second is clearly tighter, so we use it finding that $(8.4 \times 10^{-5}, 1.6 \times 10^{-4}, 2.5 \times 10^{-4})$ is below the threshold surface and therefore provides a lower bound on the point of intersection.

It is worth noting that after one level, we have left the starting ray, and have a different ratio of $p_1(\text{single}) : p_1(\text{CNOT}) : p_1(\text{Tof})$. At level 2, the ratio $p_2(\text{single}) : p_2(\text{CNOT}) : p_2(\text{Tof})$ is similar to the level 1 value because at level 1, the error rates are dominated by the failures during the error corrections, so the error rates at level 1 or higher simply reflect the number of error correction steps in each type of extended rectangle, with a small correction for the transversal gate.