

# *CMSC 411 Computer Systems Architecture*

## **Homework #3 – Unit 4 – Memory Hierarchy**

1)

- a) Assume instruction execution in the simple MIPS 5-stage pipeline, other than loads, is ideal: 1.0 cycles per instruction. If an average load takes 2.5 cycles total, and 30% of instructions are loads, what is the average CPI (cycles per instruction) of the machine?
- b) Assume a two level cache with a 99% hit rate in L1 and an 85% hit rate in L2. Hits in L1 take 2 cycles, while those in L2 take 10, and a miss in both caches that goes to memory takes 100 cycles.  
What is the average access time for this memory system, in cycles?

2)

Suppose we have a memory hierarchy with three levels of cache and also for simplicity suppose that all memory accesses are read accesses. Assume that:

TL1 is the access time of level 1 cache  
TL2 is the access time of level 2 cache  
TL3 is the access time of level 3 cache  
TM is the access time of the main memory

MRL1 is miss rate of level 1 cache  
MRL2 is miss rate of level 2 cache  
MRL3 is miss rate of level 3 cache

- a) What is the average memory access time with three levels of cache as a function of these variables?
- b) What percentage of memory accesses will result in access to the main memory?

### **3) (Challenging Problem)**

Suppose we have a memory hierarchy with 1 level of cache . Assume that:

**AT** is the average access time of cpu to memory  
**MR** is the miss rate of the cache  
**T<sub>CACHE</sub>** is the access time of the cache(whether it is read or write)  
**P<sub>DIRTY</sub>** is the percentage of cache lines that are dirty(have been modified after being filled)  
**T<sub>M</sub>** is the access time of the main memory (whether it is read or write)  
**P<sub>WRITE</sub>** is the percentage of accesses that are writes  
**P<sub>READ</sub>** is the percentage of accesses that are reads

- a) If the cache is a write-back cache, what would be the average memory access time (AT) in terms of the given variables?
- b) Answer (a) for a write-through cache instead of a write-back cache.

**4)**

Suppose we have a cache with 128 blocks, each containing 16 bytes of storage.

- a) If the cache uses direct mapping, in which cache block would the byte with address **1011 1001 1000 1011 1010 1100** reside?
- b) If the cache uses set associative mapping with an index of length 4 bits, in which set would the byte with address **1010 1001 1100 1011 0110** reside?
- c) Suppose that virtual addresses on this machine are 32 bits, and that pages are 4KB each. If the machine has 1MB of physical memory, how many standard page table entries are required if all the pages are being used? And what fraction of the pages can reside in memory at any point in time?

**5)**

Consider a Virtual Memory System with the following properties:

- 48-bit virtual address space
  - 32-bit physical address (4GB)
  - 16 Kbyte pages
- a) What is the total size of the Page Table, in bits, for each process on this machine, assuming that the Valid, Protection, Dirty and Use bits take a total of 4 bits and that all the virtual pages are being used?
  - b) The Virtual Memory system is implemented with a two-way set associative TLB with a total of 256 entries (128 sets). Describe the Virtual Memory address organization (i.e. how the address bits are partitioned for address translation) and the process of mapping an address from the Virtual Memory space to the Physical Memory space.