

# CMSC 411 : Homework #4

Due on Tuesday, March 31, 2015

*3:30pm*

**Anwar Mamat**

## Problem 1

### Cache organization

- (a) (15 points) Suppose we have a byte addressable memory of size 4GB ( $2^{32}$  bytes) with a cache of size 128KB ( $2^{17}$  bytes), not including tag bits. Also suppose the cache block size is 64 bytes. For each of the following cache organizations, compute the length in number of bits for the tag, index and offset fields of the 32-bit memory address (show your calculations):
- direct mapped
  - 2-way set associative
  - fully associative
- (b) (15 points) Given the following parameters, which performs better in terms of average memory access time, the direct mapped or the 2-way set associative cache? Assume a cache hit takes 1 cycle for either organization, and the cache miss penalty is 20 nanoseconds (both use the same memory system). Justify your answer.
- Direct mapped - miss rate 8%, 1GHz clock
  - 2-way set associative - miss rate 5%, 900MHz clock

$$\text{Average memory access time} = \frac{(\text{hit rate} * \text{hit cycles} + \text{miss rate} * \text{miss cycles})}{\text{clock rate}} \quad (1)$$

- (c) (15 points) Consider adding a fast second-level cache to a computer with only a single level cache. Suppose data can be accessed from the second level cache 8 times faster than it can be accessed from the original cache, and that the second level cache can be used 25% of the time. How much speedup can we gain by adding the second-level cache? Assume all data accesses hit in the original cache.

## Problem 2

For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-10	9-5	4-0

- (a) (8 points) What is the cache block size (in words)?
- (b) (8 points) How many entries does the cache have?
- (c) (8 points) What is the ratio between total bits required for such a cache implementation over the data storage bits?  
Starting from power on, the following byte-addressed cache references are recorded.

Table 1: Address

0	4	16	132	232	160	1024	30	140	3100	180	2180
---	---	----	-----	-----	-----	------	----	-----	------	-----	------

- (d) (8 points) How many blocks are replaced?

- (e) (8 points) What is the hit ratio?
- (f) (15 points) List the final state of the cache, with each valid entry represents as a record of [index,tag, data]

## What to submit

Submit a printed hardcopy of your solution before class starts at 3:30pm on 03/31/2015.