CNS-0509404 Update

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Project’s Recent Highlights

- Dynamic multicore reconfiguration/adaptation
  - E. İpek, M. Kırman, N. Kırman, and J.F. Martínez
    Core Fusion: Accommodating Software Diversity in Multicore Chips
    In Intl. Symp. on Computer Architecture (ISCA), June 2007
  - C.C. LaFrieda, E. İpek, J.F. Martínez, and R. Manohar
    Dynamic Core Coupling for Resilient Multicore Chips
    In Intl. Conf. on Dependable Systems and Networks (DSN), June 2007
  - J. Li and J.F. Martínez
    Power-Performance Optimization of Parallel Computing in Multicore Chips
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Challenge: CMPs Lack Flexibility

- In CMPs, core is “new transistor”
- Must support diverse apps
  - Sequential
  - Multiprogrammed
  - Parallel (coarse- or fine-grain)
  - Evolving
- Conflicting requirements
  - No. of cores
  - Per-core performance
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High-ILP, High-TLP Hardware

❖ Spatial approach: Multiscalar, RAW, Smart Memories, TRIPS
  + Modular, flexible designs
  - Significant software support

❖ Temporal approach: SMT
  + Tiny overhead on top of base core; quasi-transparent
  - Top-down approach: Large base core
    - Little tolerance for hardware bugs/faults
  - Resource interference
    - Lower parallel efficiency
Proposal: Core Fusion

- Run-time CMP “synthesis”
- High compatibility
  - Single execution model
  - Backward-compatible ISA
  - No sophisticated SW support
- Bottom-up hierarchical design
  - Tolerant to hardware bugs/faults
- No interference across base cores
  - High parallel efficiency
Contributions and Findings

❖ Run-time fully reconfigurable and distributed
  - Front-end + i-Cache
  - LSQ + d-Cache
  - ROB

❖ Thorough evaluation using diverse workload classes
  - Sequential
  - Parallel
  - Multiprogrammed
  - Evolving

❖ Effective
  - Always best or 2\textsuperscript{nd} best
  - Always best in intermediate parallelization stages
  - Others lag significantly in 1+ cases

❖ Highly compatible
Conceptual Organization

- Concept: Add enveloping hardware to enable on-demand core fusion

Not meant to represent actual floorplan
Core Fusion Operation

- i-Cache fusion and reconfiguration
- Collective fetch
- Instruction steering/renaming
- Collective execution
- Distributed memory access
- Collective commit
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Collective Fetch
Collective Fetch
Collective Commit I

Pre-commit

Commit
Collective Commit II

Pre-commit: i0, i1, i2
Commit: i0, i2
Run-time Reconfiguration

- Run-time control of granularity
  - Serial vs. parallel sections
  - Variable granularity in parallel sections
- Mechanism: Fusion, fission ISA instruction
  - Typically encapsulated in macros or directives (e.g., OpenMP sections)
  - Can be safely ignored (single execution model)
- Relatively simple
  - Flush pipelines and i-caches
  - Reconfigure i-cache tags
  - Transfer architectural state as needed
Evaluation Nugget: Evolving Apps

Evolving Application Performance (MG)

Speedup Over Stage Zero Run on FineGrain-2l

- FineGrain-2l
- Core Fusion
- CoarseGrain-4l
- CoarseGrain-6l
- Asymmetric-4l
- Asymmetric-6l

stage0 stage1 stage2 stage3
Issues that Intrigue Me

- Synergistic hardware-software technology
  - Virtualization
  - OS scheduling
  - Multicore compiler mechanisms
  - Application programming
Acknowledgments

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    - CCF-0429922 (Pinkston)
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NGS-CSR Workshop Bullet

❖ If we forget Amdahl’s Law, it will come back to haunt us