Problem Set #8

Quantum Error Correction
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Due Tues., March 13, 2007

Problem #1. Fault-Tolerance With SWAPs Within a Code Block

As mentioned in class, one approach to dealing with nearest-neighbor gates is to perform SWAPs to move qubits to where they are needed. SWAPs do not propagate errors, but a single faulty SWAP gate can cause two errors, possibly in the same block of the code. We investigate fault-tolerance under this possibility.

a) Modify EC properties 1 and 2 and gate properties 1 and 2 (for a code that corrects t errors) in order to allow gadgets where one faulty location during the gadget can cause two errors in the same code block. (But we don't allow any greater error propagation than before.) In particular, we want definitions where the usual fault-tolerant constructions will work when the qubits are moved around with SWAP gates which may interact qubits within a single code block.

b) Show that if we use a code correcting $t = 2$ errors but still require that a "good" extended rectangle contains at most one faulty location, then a good extended rectangle satisfies the same correctness property as before. (You may show it only for the case of a gate extended rectangle.)

c) Now consider an error model where there is additional source of errors that affects neighboring pairs of physical qubits regardless of whether or not there is a gate between them. Assuming that a single fault in a gadget could be either a faulty location in the old sense or one of these additional two-qubit errors, show that the properties from part a still apply.

   Describe the behavior of the SWAP gate error model and the two-qubit correlated error model under concatenation. How is it unusual compared to the situation we considered in the lecture? Note any differences between the SWAP gates and two-qubit correlated errors in the behavior under concatenation.

Problem #2. Pseudothresholds for Fault-Tolerance

For this problem, we will study the classical reversible concatenated fault-tolerant circuits from problem 2 on problem set 7 when we allow different error rates for the different types of gates. In order to keep everyone on the same page, assume the fault-tolerant error correction circuit is the one from the solution set, i.e., it has 6 state preparations, 12 waits, 12 CNOTs, and 3 Toffoli gates.

a) Let us lump together bit preparations, waits, and single-bit gates (i.e., the NOT gate) for simplicity. Find the failure probability of extended rectangles (that is, the probability of the rectangle being bad) for single-bit operations, CNOTs, and Toffoli gates in terms of $p_0(\text{single})$, $p_0(\text{CNOT})$, and $p_0(\text{Tof})$, the error rates for physical single-bit operations, CNOTs, and Toffolis, respectively. (Remember to use the largest extended rectangle for the different types of locations lumped into single-bit operations.)

b) Assume that the physical (unencoded) error rates satisfy $p_0(\text{single}) = p$, $p_0(\text{CNOT}) = 2p$, and $p_0(\text{Tof}) = 3p$. A *pseudothreshold* for a given level j of encoding and given type R of extended rectangle is defined to be the error rate $p_T(j, R)$ for which $p_0(R) \leq p_T(j, R)$ implies that $p_j(R) \leq p_0(R)$ (where

$p_j(R)$ is the failure rate of the extended rectangle of type R under j levels of concatenation). It is generally sufficient to find $p_T(j, R)$ by solving the equation $p_0(R) = p_j(R)$.

Find the pseudothresholds for the three types of extended rectangles with one level of encoding.

c) Under the same assumption in part b, calculate the pseudothresholds for the three types of extended rectangles with two levels of encoding. Note that the pseudothresholds at level 2 are different from the values at level 1 — this is why they are just pseudothresholds and not true thresholds. In general, the pseudothreshold for a given type of extended rectangle may increase or decrease with level.

d) When we let the error rates be different for different physical gates, there is no longer a threshold value but a threshold *surface*, the boundary of the region (in this case, a 3-dimensional region) for which the set of physical error rates leads to arbitrarily low logical error rates at high levels of concatenation. In order to study the threshold surface, we frequently look at rays from the origin with a fixed ratio of error rates for the various gates, such as the $1 : 2 : 3$ ratio used in parts b and c. For a particular ray, we are then interested in the point of intersection of that ray with the threshold surface. The coordinates of that point will then determine a set of simultaneous thresholds for the various gates — if all gate error rates are below these values, then concatenation will drive the logical error rates to 0.

Use the results of part b and/or c to set lower bounds on the coordinates of the points where the $1 : 2 : 3$ ray intersects the threshold surface.