K-maps and Sequential Circuits

250H

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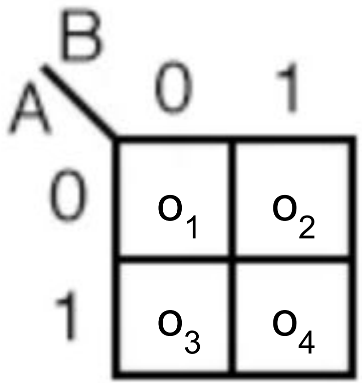
- The problem of getting the BEST circuit is thought to be hard

K-maps for 2 Variables

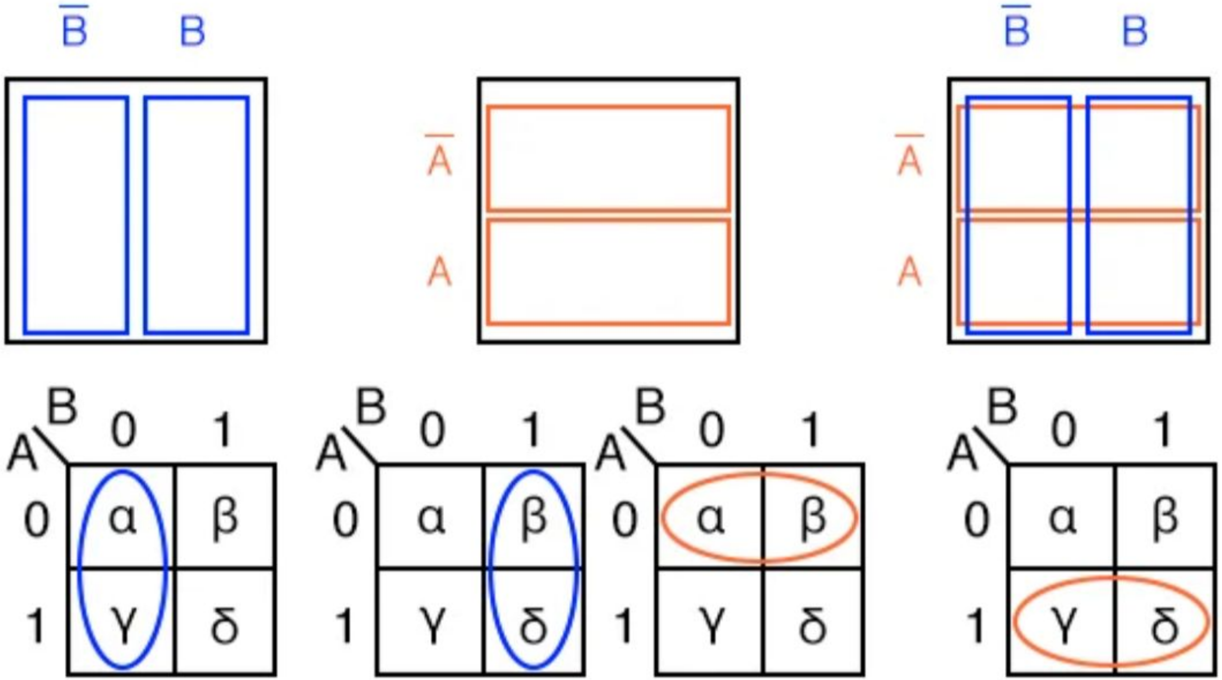
- The outputs of a truth table correspond with a Karnaugh map entries



A	B	Output
0	0	o_1
0	1	o_2
1	0	o_3
1	1	o_4

K-maps for 2 Variables

- We can simplify the expression by using the regions shown here



K-maps for 2 Variables Example

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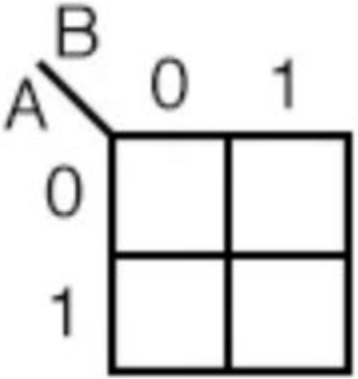

A	B	Output
0	0	0
0	1	1
1	0	0
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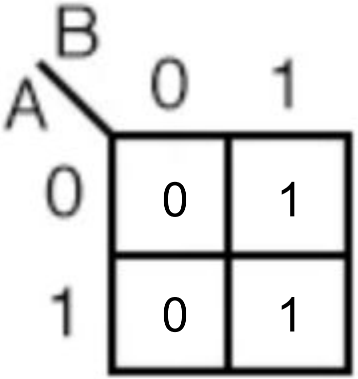

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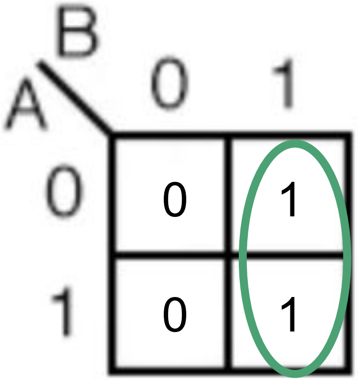

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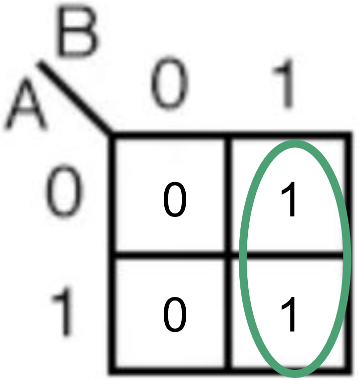

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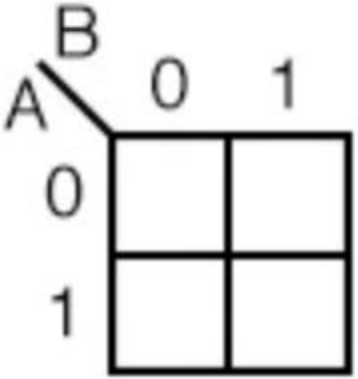

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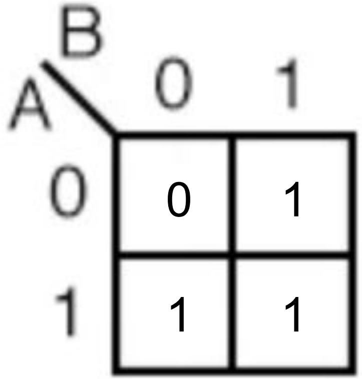

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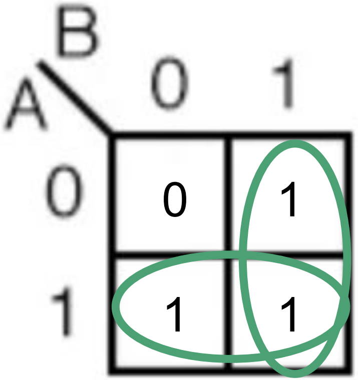

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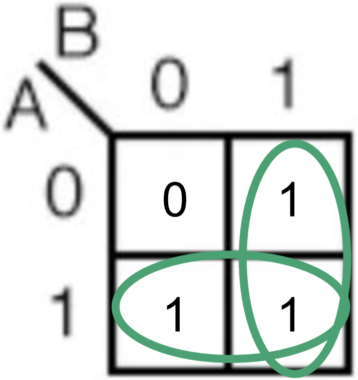

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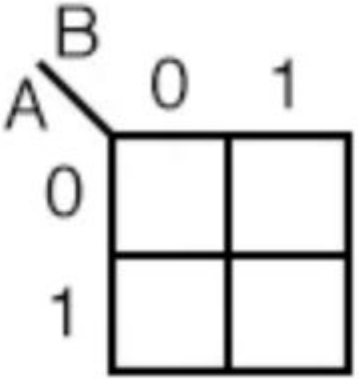

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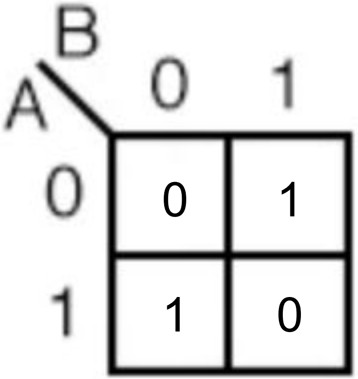

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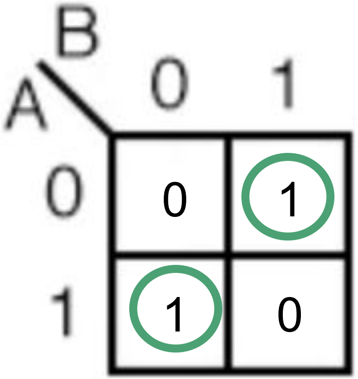

A	B	Output
0	0	0
0	1	1
1	0	1
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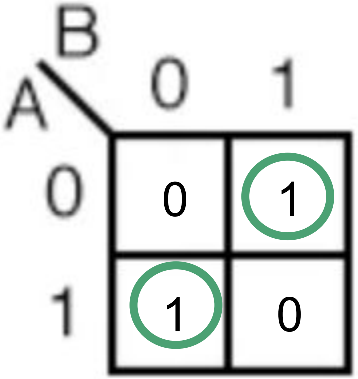

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  - $\overline{A}B + A\overline{B}$
- We first translate the table to our k-map
- We now want to look at the relationships of the 1's
- Since we see that we have nothing in common the simplest we can make this statement is
  - $\overline{A}B + A\overline{B}$

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

K-maps for 3 and 4 Variables

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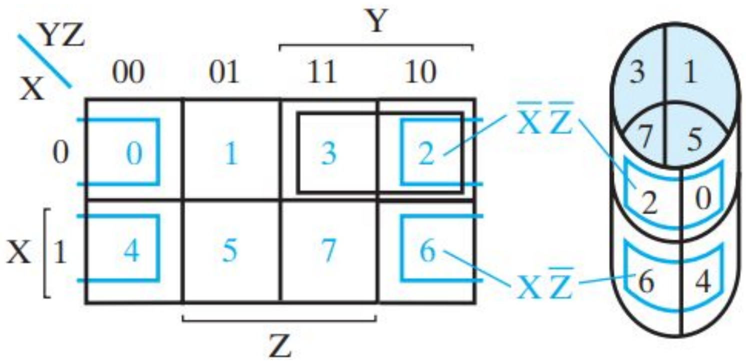
Three Variables:



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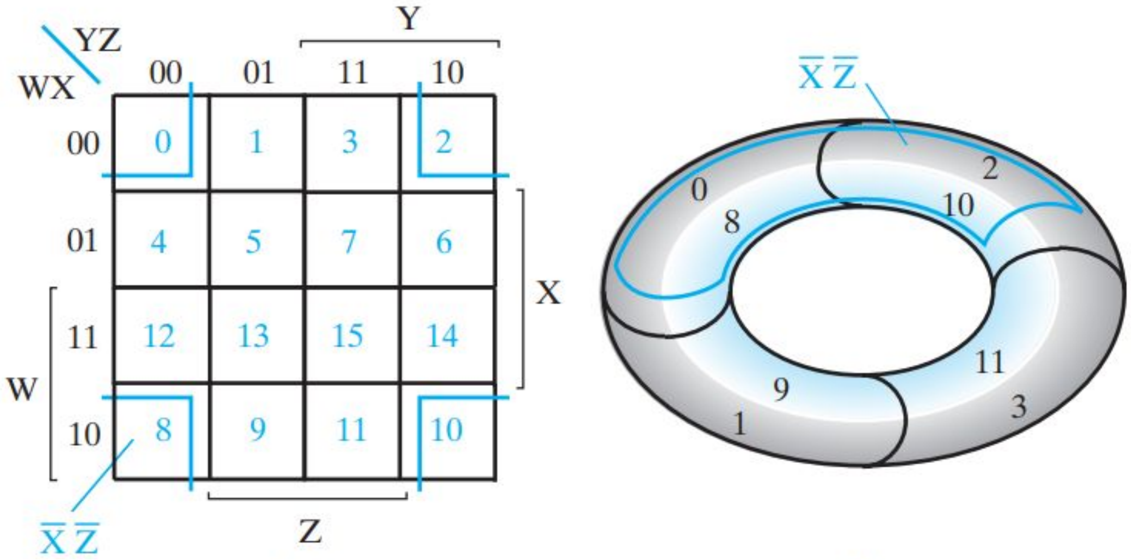
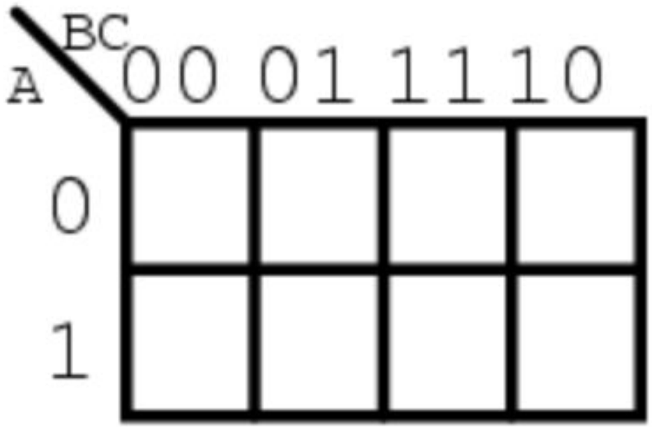
Four Variables:



K-maps for 3 Variables Example

A	B	C	Output
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0



K-maps for 3 Variables Example

A	B	C	Output
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

A \ BC	00	01	11	10
0	1	1	1	1
1	1	1	0	0

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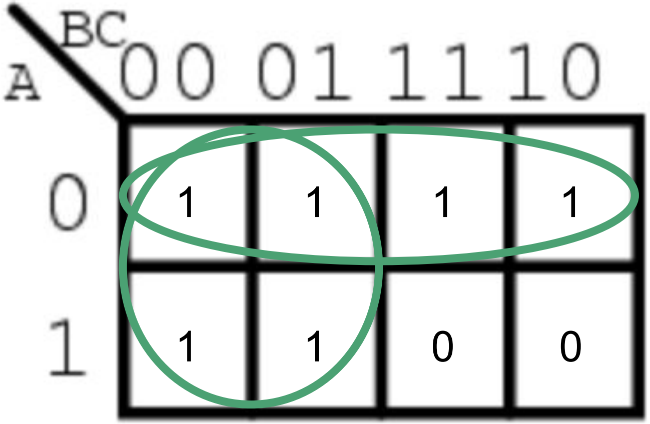
A	B	C	Output
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0



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0	0	0	1
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1	0	1	1
1	1	0	0
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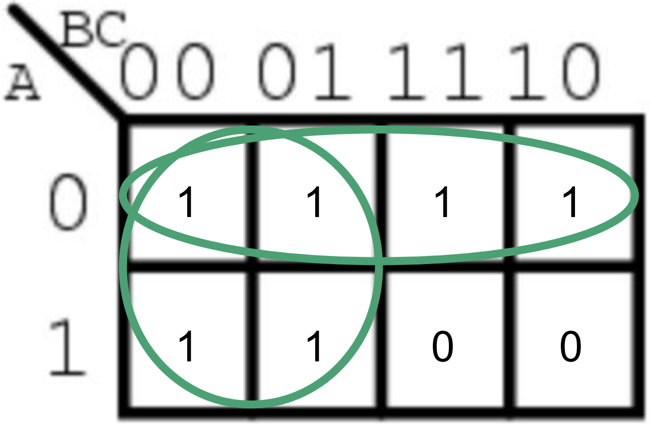

Output: $\overline{A} + \overline{B}$

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0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
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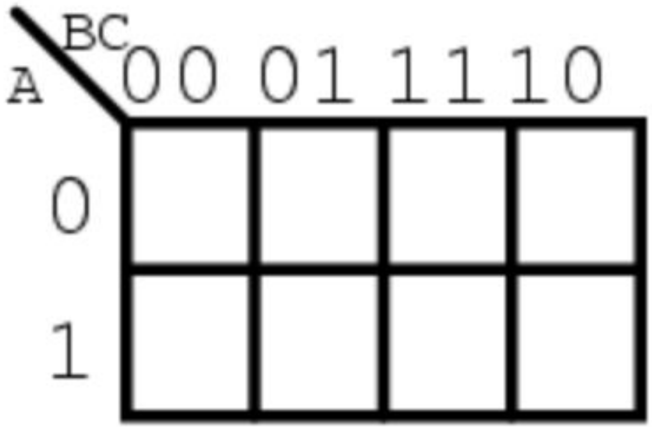

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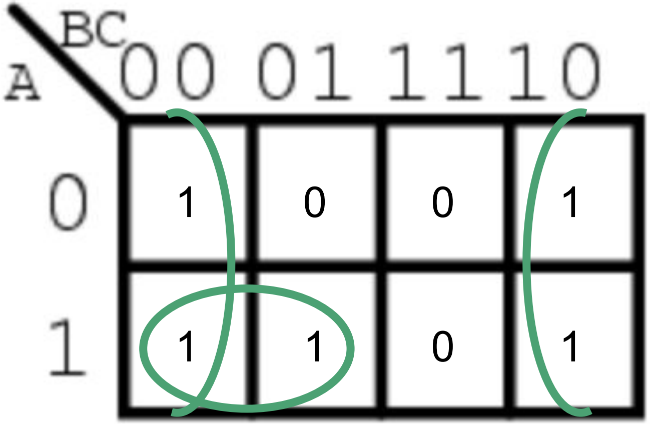

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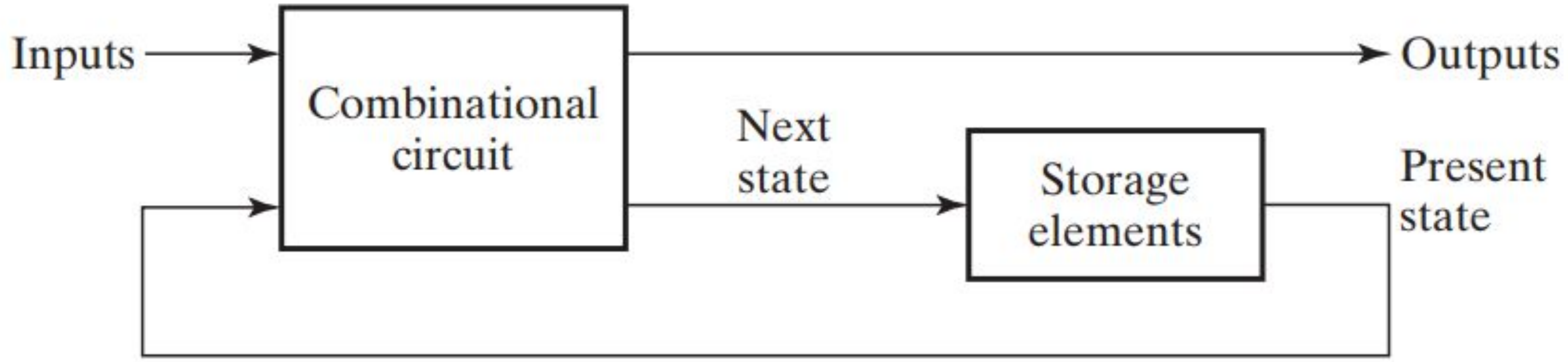
- These storage elements are described as sequential circuits



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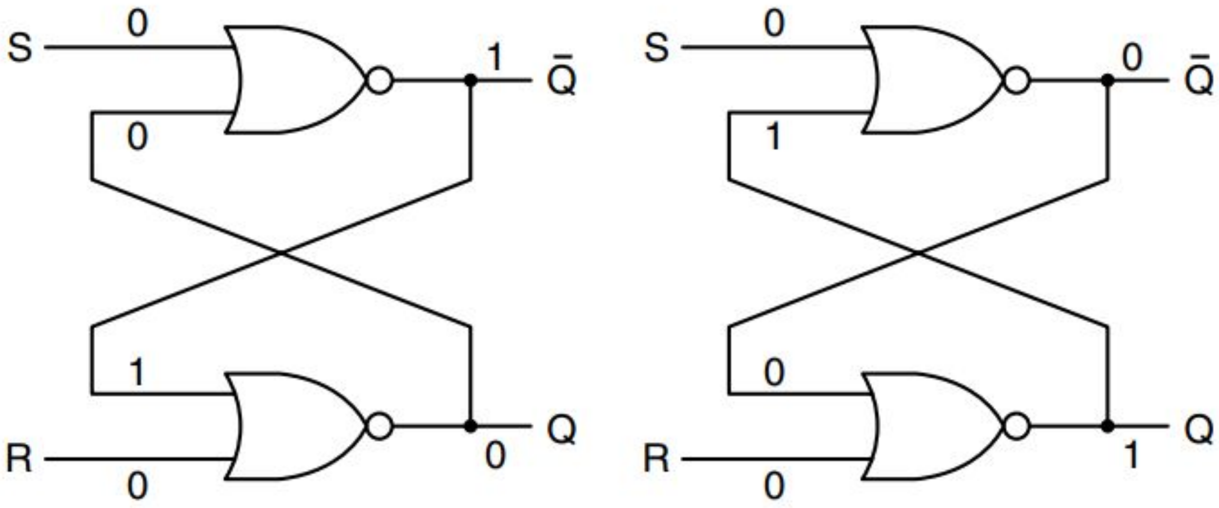

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- Using this property, we can build computer memories

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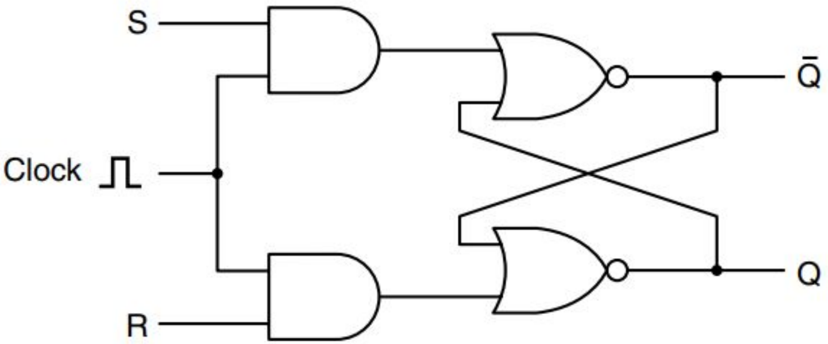

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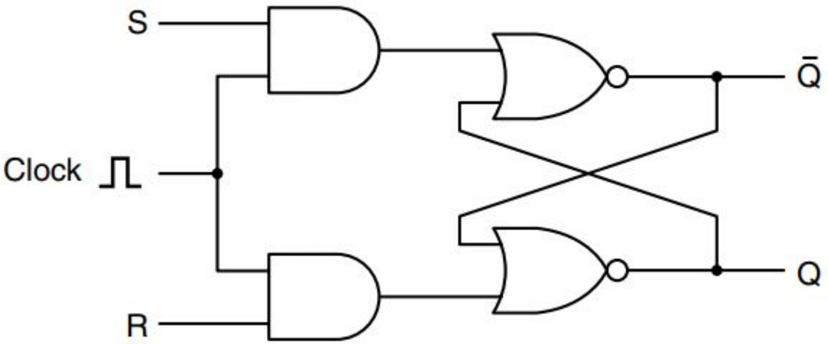

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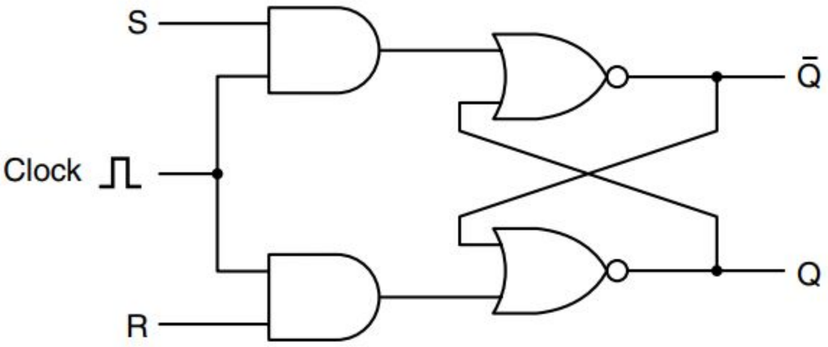

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- With the clock 0, both AND gates output 0, independent of S and R, and the latch does not change state
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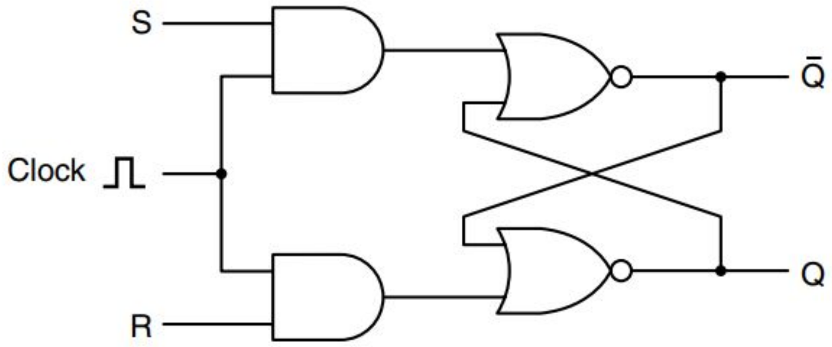

Clocked D Latch

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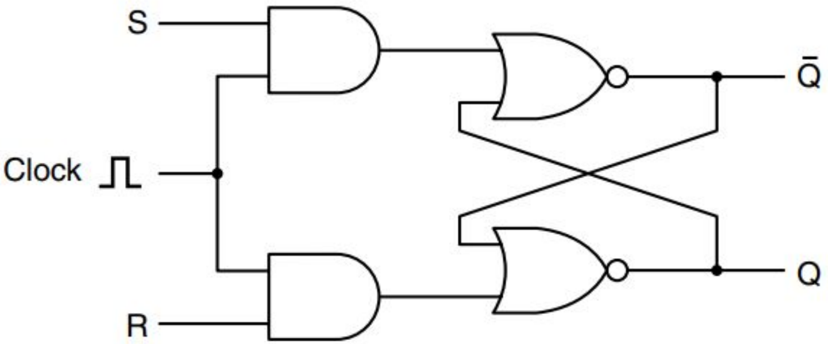

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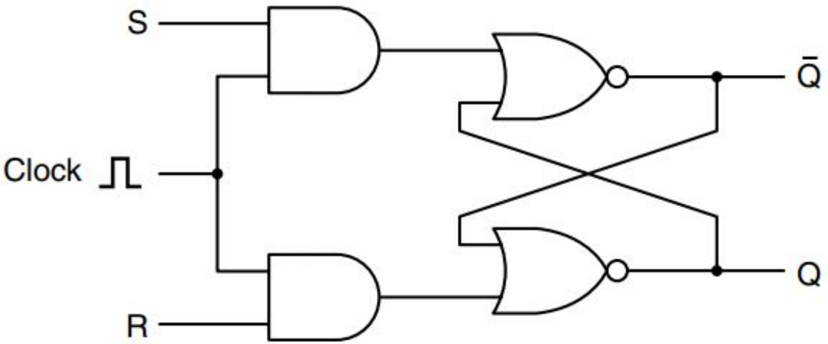

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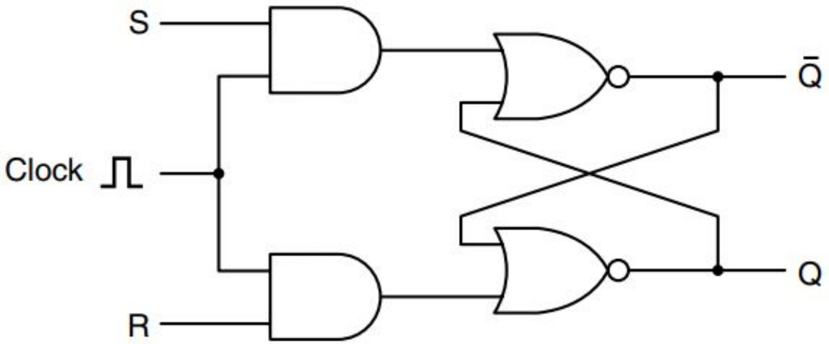

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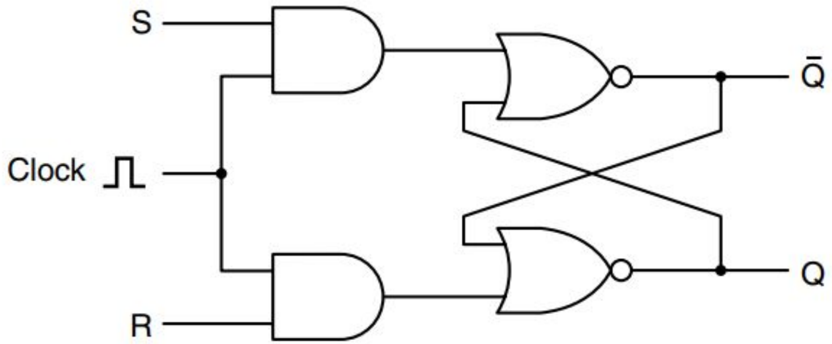
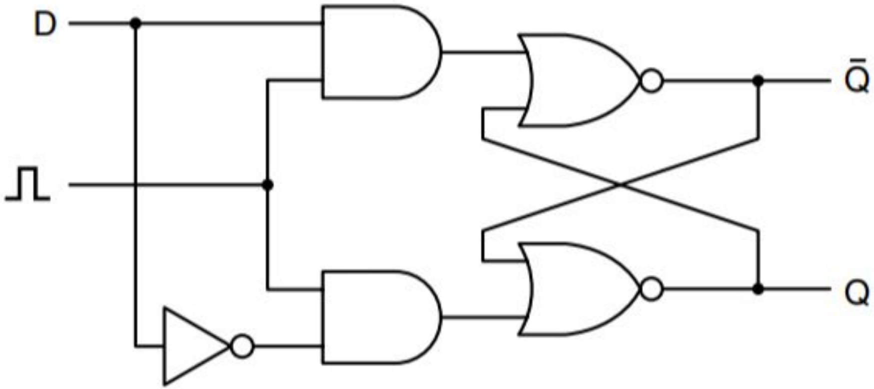
- The latch will jump to one of its stable states at random



Clocked D Latch

- We resolve this issue by preventing it from ever happening
- We create a circuit that only has one input: D
- Because the input to the lower AND gate is always the complement of the input to the upper one, the problem of both inputs being 1 never arises.



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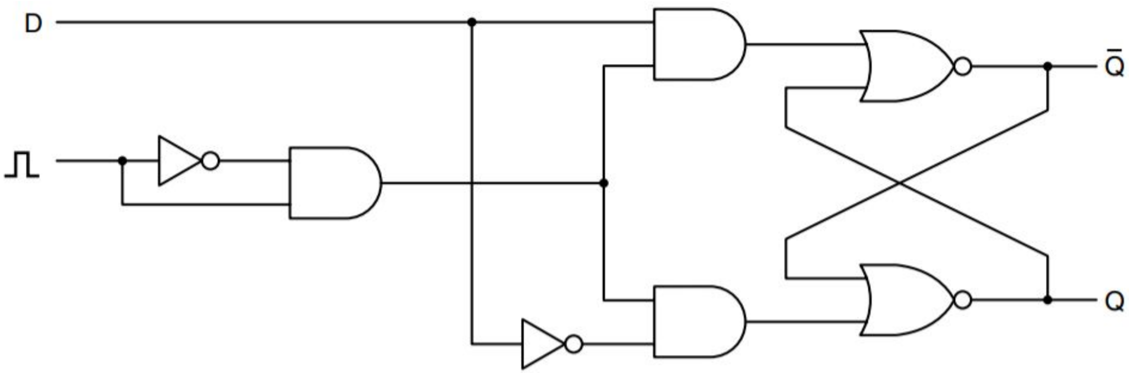

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- The register accepts an 8-bit input value when the clock transitions
- To implement a register, all the clock lines are connected to the same input signal
- Each register will accept the new 8-bit data value on the input bus