Solution V

5-3

0010, 1001, 0100, 1010, 1101, 0110

5-4

Serial data is transmitted one bit at a time. Parallel data is transmitted in groups of n bits (n > 1) Serialdata can be converted into parallel data by entering it into a shift register one bit at a time until n bits are entered and then reading out the register. Parallel data can be converted into serial data through the use of a shift register with parallel load. The data is loaded into the register and then the n bits are shifted out of the register serially, one bit at a time.

5-5

Time:	0	1	2	3	4
A	0101	0010	0001	0000	1000
B	0011	0001	0000	0000	0000
C	0	1	1	1	0

5-7

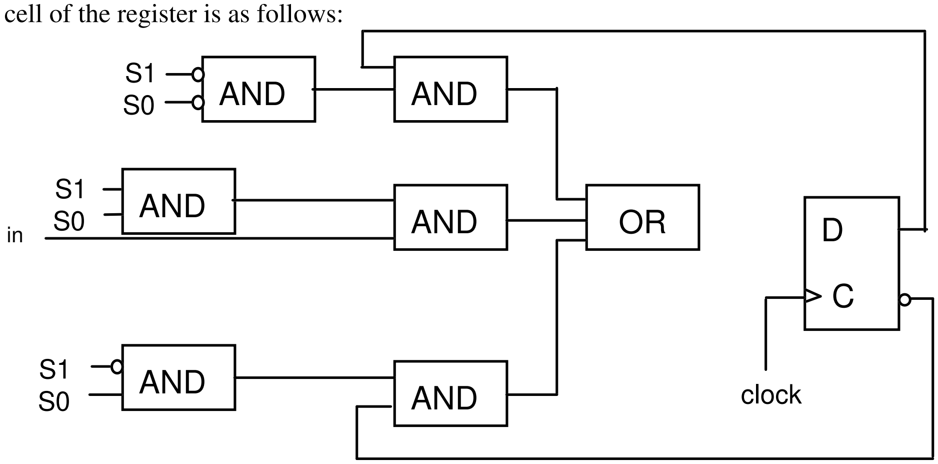
Replace each AND gate in Figure 5-6 with an AND gate with one additional input and connect this input to the following:

(SHIFT)(AND)

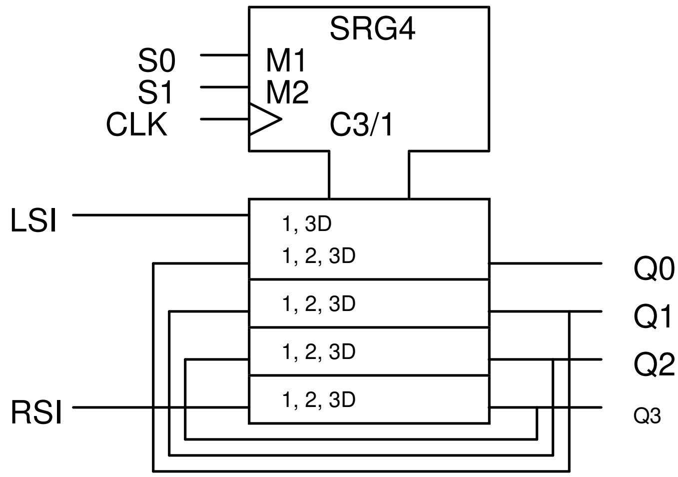
This will force the outputs of all the AND gates to zero, and on the next clock edge the register will be cleared in LOAD and SHIFT are logic one.

5-8

The basic cell of the register is as follows:



5-10



5-12

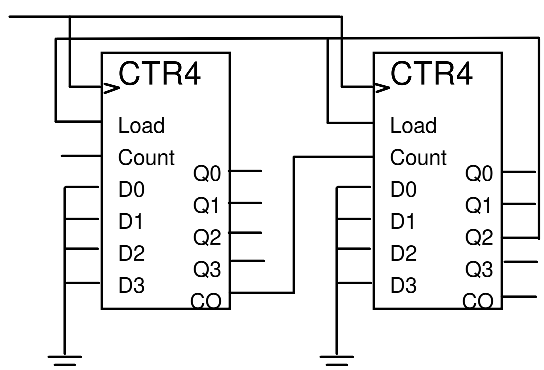
Max Delay = 12 (4ns) = 48 ns
f = 1/T = 1/48 ns = 20.83 Mhz

5-16

Present state	Input	Next state	FF Input
A	X	A	Y
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

$Y = A \oplus X$

5-21



5-24 a

$J_A = BC$
$K_A = 1$
$J_B = C$
$K_B = C$
$J_C = A'$
$K_C = 1$

5-26

Present state				Next state				FF Inputs			
A	B	C	D	A	B	C	D	D_A	D_B	D_C	D_D
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	1	0	0	0	1	0	0
0	1	0	0	1	0	0	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0

$D_A = b$
$D_B = C$
$D_C = D$
$D_D = A'\ B'\ C'\ D'$