Integrating Electrical and Mechanical Design and Process Planning

*S. J. J. Smith**
Hood College
Department of Mathematics and Computer Science, Hood College, 401 Rosemont Avenue, Frederick, MD 21701-8575, USA

K. Hebbar,† D. S. Nau,‡ and I. Minis§
University of Maryland
Institute for Systems Research, University of Maryland, College Park, MD 20742, USA

Abstract

This paper reports on the development of the process-planning module for EDAPS, an integrated system for designing and planning the manufacture of microwave modules. Microwave modules are complex devices having both electrical and mechanical properties, and EDAPS integrates electrical design, mechanical design, and process planning for both the mechanical and electrical domains.

EDAPS's process planning module provides an integrated approach to process planning in both the electronic and mechanical domains, specifically in the manufacture of microwave transmit-receive (T/R) modules. It enables EDAPS to generate process plans concurrently with design—and we are developing ways for EDAPS to use the process planning information provide feedback to designers about manufacturability, cost, and lead time for manufacturing their designs.

The planning module is based on a modified version of an AI planning methodology called Hierarchical Task Network (HTN) planning. We provide an overview of its operation, and compare and contrast it to how HTN planning is normally done.

Keywords

Computer aided design, concurrent engineering, process planning, systems integration, electronic manufacturing, microwave module.

---

*Also in the Institute for Systems Research and the Department of Computer Science, University of Maryland. Telephone 301-696-3729; fax 301-694-7653; email `sjsmith@nimue.hood.edu`.

†Also in the Department of Mechanical Engineering. Telephone 301-405-6572; fax 301-405-6707; email `hebbar@isr.umd.edu`.

‡Also in the Department of Computer Science. Telephone 301-405-2684; fax 301-405-6707; email `nau@cs.umd.edu`.

§Also in the Department of Mechanical Engineering. Telephone 301-405-5310; fax 301-405-6707; email `minis@isr.umd.edu`.

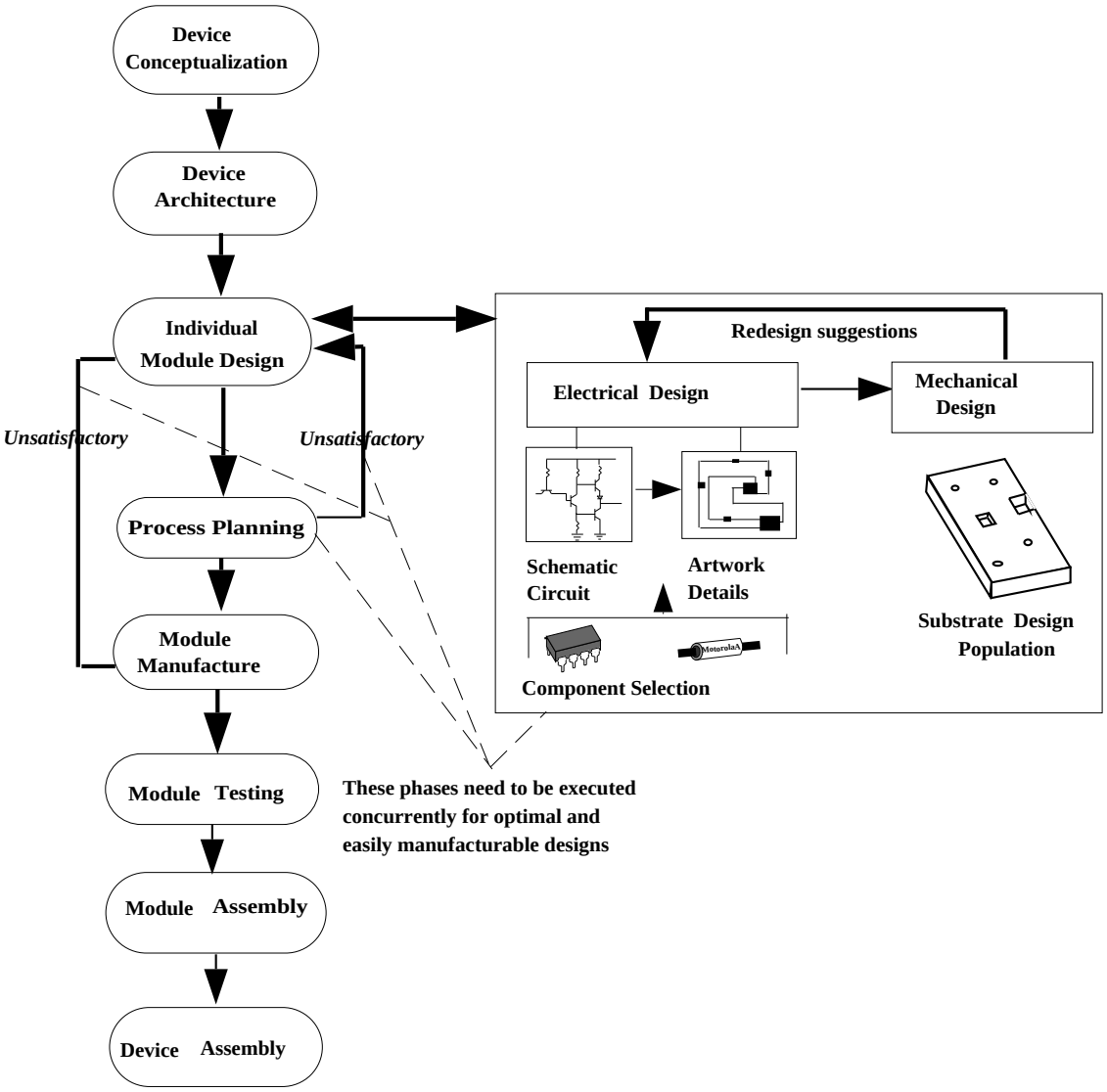

Figure 1 Design and manufacturing cycle for microwave T/R modules.

1 MOTIVATION

In [20], we argued that although AI planning techniques can potentially be useful in several manufacturing domains, this potential cannot be realized without developing more realistic and more robust approaches to issues important to manufacturing engineers. We further argued that by looking realistically at issues important to manufacturing engineers, AI researchers might be able to discover principles relevant for AI planning in other domains. This paper attempts to address both of these objectives, in a manufacturing planning domain quite different from the machining domain described in [20]: the design and manufacture of complex electro-mechanical devices. More specifically, this paper focuses on the use of AI planning techniques for process planning in the design and manufacture of *microwave transmit-receive (T/R) modules* (described further in Section 3).

Figure 1 illustrates the design and manufacturing cycle for microwave T/R modules,

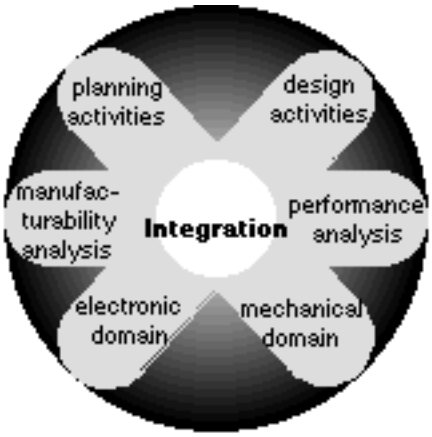

Figure 2 Integration of disciplines for the design and manufacture of complex electromechanical devices.

which is highly interdisciplinary in nature. Electronic designers develop the detailed circuitry; mechanical designers design the device to resist shock and vibrational loadings, and develop the assemblies, the heat removal systems, and the housing of the device; and manufacturing engineers apply electronic manufacturing processes (such as lithography, soldering, cleaning, and testing), and mechanical manufacturing processes (such as drilling and milling) to manufacture the end product.

For many manufactured products, the decisions made during the design of the product will determine most of the cost of manufacturing the product. This has given rise to the philosophy of *integrated product and process design* (IPPD), which attempts to take manufacturing considerations into account while the product is being designed. However, in the design of a complex product, this requires coordinating a large interdisciplinary team. In large organizations, this can be a difficult task [21].

The task of communicating design and manufacturing requirements and design changes across disciplines could be greatly aided by a carefully designed computer system that integrates both electronic and mechanical computer-aided design (CAD) tools, and provides access to process planning and design evaluation capabilities, as shown in Figure 2. Such a system could be used for designing both the electronic and mechanical aspects of a product, analyzing various aspects of the design's performance, planning how to manufacture the proposed design, and evaluating the process plans to provide feedback to the designers about the design's manufacturability.

Few existing computer systems can successfully address all of these issues in a single integrated environment—and there are several open questions about the best way to design such a system. To explore these issues, we have created the *Electro-mechanical Design And Planning System (EDAPS)*, a toolkit for microwave T/R module manufacture that integrates electronic and mechanical computer-aided design, electronic and mechanical process planning, and plan-based design evaluation. EDAPS's process planning module generates process plans concurrently with design, and assists the designers in performing plan-based critiquing of microwave T/R module designs.

EDAPS incorporates electronic design, mechanical design, and process planning modules into a single integrated environment. Its process planning module plans both in the mechanical domain, including such processes as drilling and milling, and in the electronic

domain, including such processes as via plating, artwork deposition, component placement, and soldering. This allows EDAPS to provide feedback about manufacturability and lead time to the designers, based on process plans for the manufacture of the device.

2 RELATED RESEARCH

Manufacturability analysis for mechanical designs. Jakiela *et al.* [16] have built a rule-based Design-For-Assembly system that gives feedback about assemblability when the designer adds new features to the design. Another rule-based manufacturability system was developed by Ishii [15]. Our IMACS system [10] generates the best operation plans for machined components and gives feedback about manufacturing infeasibilities in the design. However, none of these tools are applicable to the electronic domain.

Manufacturability analysis for electronic designs. Commercially, several CAD tools are available for electronic circuitry design (such as Mentor Graphics, OrCAD, EEsof, and MAGIC). These electronic CAD packages automatically check design rules, and some even perform manufacturing yield analysis of the design. However, since these packages use a two-dimensional representation of the design, they neither represent three-dimensional mechanical features nor perform any sort of mechanical feasibility and manufacturability analysis on devices. Such tasks would require a three-dimensional solid-model representation of the design. Harhalakis *et al.* have developed a rule-based system for critiquing the manufacturability of microwave modules [11], but it is not directly linked to an electronic or mechanical CAD system. Feldmann *et al.* [8] describes a system that integrates electronic and mechanical CAD tools for three-dimensional molded printed circuit boards, where circuits are no longer in planar configurations. However, these tools and systems do not evaluate the designs with respect to cost and lead times.

Computer-Aided Process Planning. Most CAPP systems work only for purely mechanical products; [26] gives a comprehensive review of such systems. A few efforts (e.g., [25, 18]) have focused on CAPP for electronic applications, but these systems do not incorporate many manufacturing processes in the mechanical engineering domain. For electromechanical designs, Candadai *et al.* [4] use a Group-Technology-based approach to generate high level process plans in both domains for the manufacture of these designs, but this system does not work concurrently with an electronic CAD tool.

Design Integration. The DARPA/MADE program focuses on achieving IPPD goals in the manufacture of Complex Electro-Mechanical (CEM) devices [31]. CEM devices, such as optical cameras and CD-ROMs, are more complex than the devices considered in this paper. As part of MADE, the SHARE project [29] examines how information technology tools could be applied to promote collaboration between design teams.

Tradeoff Analysis. The MSDA advisor [23] evaluates system level trade-offs between physical size, weight, thermal characteristics, reliability, cost, performance, and so forth in the selection of packaging technologies for components used in PCBs and ceramic substrates. The EXTRA system [2] does tradeoff analysis for selecting alternative components and subassemblies for microwave modules.

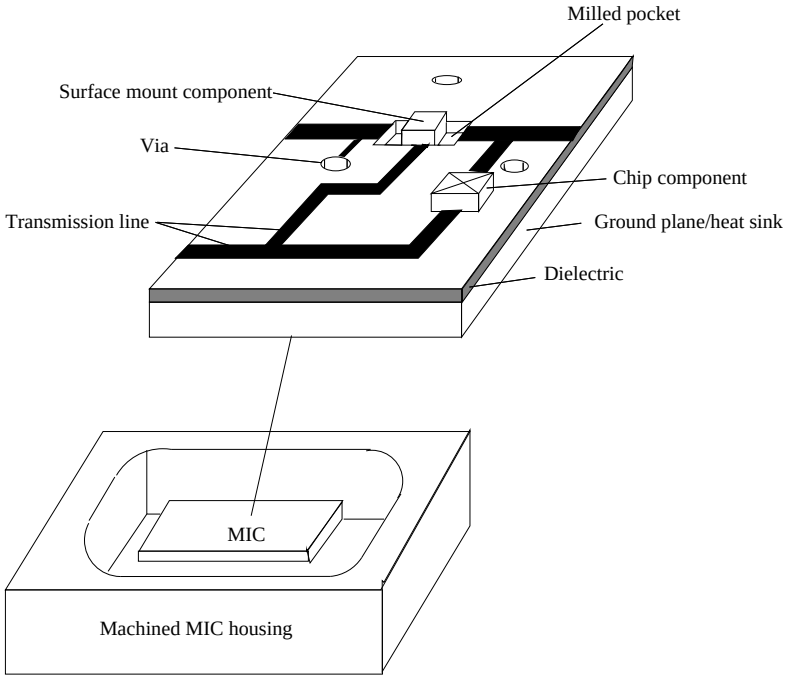

Figure 3 A typical microwave T/R module, consisting of the MIC substrate, and its housing.

3 MICROWAVE T/R MODULES

3.1 Introduction

Most commercial electronic products operate in the 10kHz–1GHz radio frequency (RF) spectrum. However, in the telecommunications arena, the range of operating frequencies has been increasing at a tremendous pace. For scientific and commercial long-range defense applications—such as radar, satellite communications, and long-distance television and telephone signal transmissions—radio frequencies prove unsuitable, primarily due to the high noise-to-signal ratio associated with radio frequencies. Moreover, the lower-frequency bands have become overcrowded due to the overuse of these bands for commercial communications applications [30].

Consequently, in contrast to other commercial electronic products, most modern telecommunications systems operate in the 1–20 GHz microwave range, and *transmit/receive (T/R)* modules of such systems are termed *microwave T/R modules* (see Figure 3). Microwave design is different from RF design in that the transmission lines that carry the signals have distributed impedances associated with them. Therefore, the shape and dimensions of transmission lines, which are unimportant in RF designs, are critical to microwave designs. These new requirements impose new challenges on the design procedure.

3.2 Terminology

In earlier microwave circuit assemblies, different parts of the circuit were built separately using *coaxial cables* or *waveguides*, and later assembled by screwing the parts together.

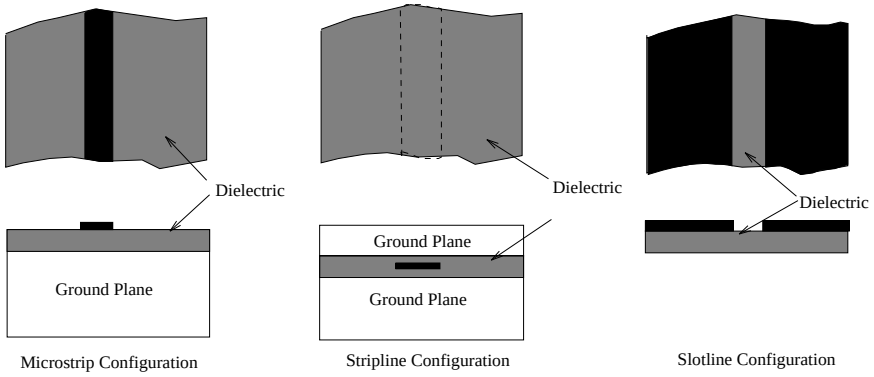

Figure 4 Transmission lines in microwave manufacturing.

Owing to the size and configuration of the coaxial cables and waveguides, the assemblies were significantly large, and the assembly procedure was time-consuming and clumsy. These earlier assemblies were replaced by *Microwave Integrated Circuits (MICs)*, where all functional components of the circuit are fabricated as *artwork* on the same planar board, using the same fabrication technology. In MICs, functional components such as transistors, resistors, and capacitors can be classified as either "integrated" or "hybrid". *Integrated* components are fabricated as a geometric manifestation of the artwork. *Hybrid* components are assembled separately using techniques such as soldering, wire bonding, and ultrasonic bonding.

MIC technology resulted in a reduction of the size of manufactured devices by several orders of magnitude. In MICs, the manufacture and assembly stages of manufacturing a circuit are integrated, and thus the lead time for manufacturing is reduced. The next level of integration has been achieved by *Monolithic Microwave Integrated Circuits (MMICs)*, in which all functional units, including the lumped elements, are fabricated as artwork on a single planar board. In this work, we consider the manufacture of MICs only.

We will use these terms throughout the paper (see Figure 3 and Figure 4):

- The *dielectric* is the substrate on which the artwork is laid out, and on which the hybrid components are assembled. The dielectric serves as a wave-conducting medium. Common materials used are PTFE (Teflon), polyolefin, and aluminum-oxide ceramic.
- The *ground plane* is a metallic layer on top of which the dielectric layer resides. The ground plane is usually made of copper or aluminum. It provides grounding for the circuit and mechanical strength for the device, and it acts as a medium to conduct away heat generated by the device. The heat flux of components in MICs, especially those that transmit power to transmitters, is generally very high, on the order of 10-1000 MW/cm^3 [24]. Therefore, heat sinking is critical to the performance of the device. The ground plane is the mounting surface for the hybrid components. Thus, machined features such as milled pockets and drilled holes are developed on the ground plane.
- The *artwork* is an etched circuit pattern containing traces, pads to mount hybrid components, components that are directly fabricated on the circuit, fiducials, and reference text elements. Usually, the artwork forms the topmost layer of the dielectric.
- *Transmission lines* are traces that carry energy to different parts of the circuit. Figure 4 illustrates several possible configurations of transmission lines. The Microstrip configuration is the simplest to manufacture.

- *Vias* are through-holes in the dielectric that connect the upper layer to bottom of the ground plane. Vias also conduct heat from the upper artwork layers to the heat sink.
- *Surface-mount components* are hybrid elements that are assembled on the surface of the dielectric. The leads of these components do not go into the dielectric (as opposed to the leads of through-hole components, which go through the surface). Surface-mount technology is quickly replacing through-hole technology because of the reduction in size and the ease of automating the manufacturing processes.
- *Mounting features* are usually milled pockets that are used as recesses in which surface-mount components will sit. These pockets are especially necessary for components that dissipate high heat, because these components need to be directly connected to the heat sink. Such components include Gunn diodes and Impatt diodes.
- The *housing* is a cast, or machined, metallic enclosure which envelopes the entire assembled device. These enclosures are needed to provide electronic isolation of the devices; to provide rigidity and strength; to make external connections easy; and to dissipate the heat conducted from the device heat sinks.

3.3 Electronic Manufacturing Processes

The production method used for MICs depends on several factors, such as the choice of dielectric material and the degree of integration of functional elements in the design. If all elements are assembled as hybrids, then lamination, photomask deposition, etching, plating, adhesive deposition, application of flux, reflow soldering, trimming, cleaning, testing, tuning, drilling, milling, and casting form a superset of the operations used [5, 3]. If, however, some components are fabricated as integrated elements, thin film and thick film deposition techniques must be used in addition [13]. In this work, we assume that the modules are fabricated as hybrid-only microstrip MICs, so that the thin/thick film processes can be avoided.

4 SYSTEM ARCHITECTURE

In the EDAPS system, we want to provide the designers with CAD tools for electronic and mechanical design, and with an integrated process planner for manufacturing processes in both the mechanical domain and the electronic domain. Thus the EDAPS system consists of three modules that can be invoked from a common user interface (see Figure 5):

- In EDAPS's *circuit schematic and circuit layout module*, the designers generate electronic circuitry. On top of an integrated set of packages supplied by EEsof's Series IV [6] software, which forms the core of this module, we have developed routines to provide us with application-specific information. We address this module in more detail in [12].
- In EDAPS's *substrate design module*, the designers develop mechanical features of the MIC. Bentley Systems' Microstation CAD software application [19] supplies the set of tools required to achieve this functionality. The ACIS [1] solid modeler is used internally to represent and provide methods to generate and modify features defined in Microstation. We are developing routines in C++ and the Microstation Development

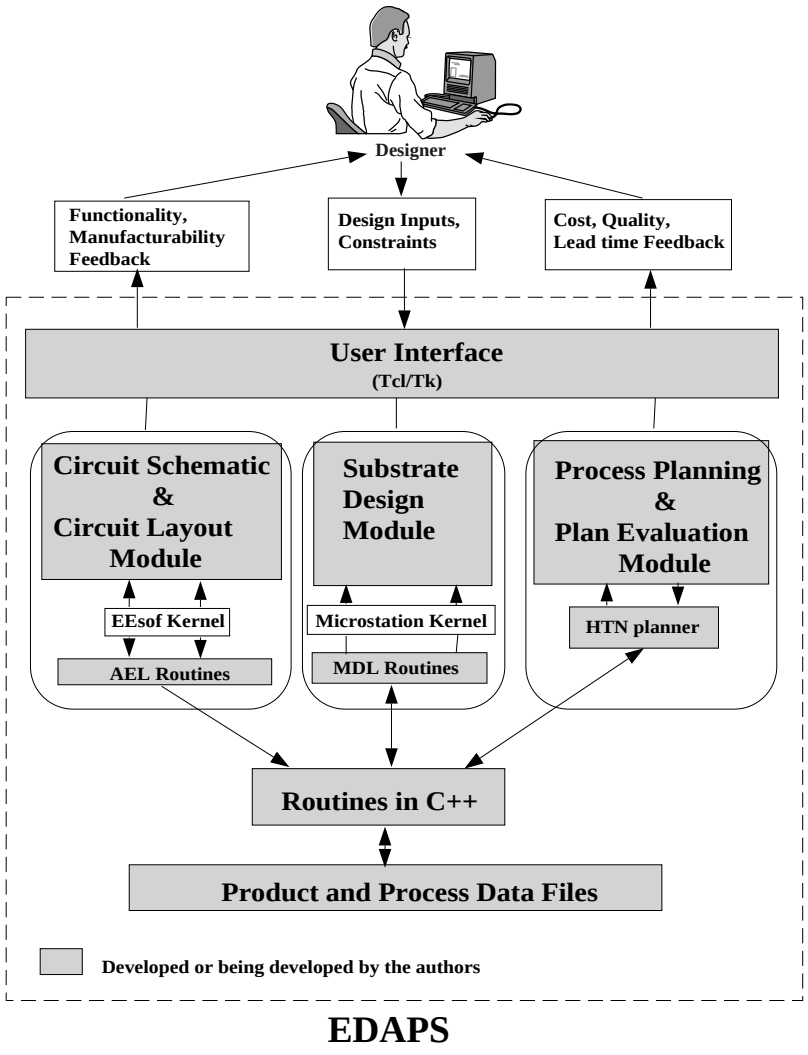

Figure 5 System architecture.

Language to integrate Microstation with the rest of the system and to extract and supply relevant manufacturing information. More details are available in [12].

- EDAPS's *process planning module*, which is the subject of this paper, creates a process plan for the design, and reports the lead time for the design to the designers. The process planning module is described in more detail in Section 5.
- The coordination of these modules and the exchange of data among them takes place through a user interface written in the *Tcl/Tk* language [22]. This user interface allows the designers to smoothly interact with the heterogeneous modules of the system.

5 PROCESS PLANNING AND PLAN EVALUATION MODULE

To perform process planning for microwave T/R module designs, we use techniques from *hierarchical task-network (HTN)* planning [32, 33, 7]. We have also used this approach in

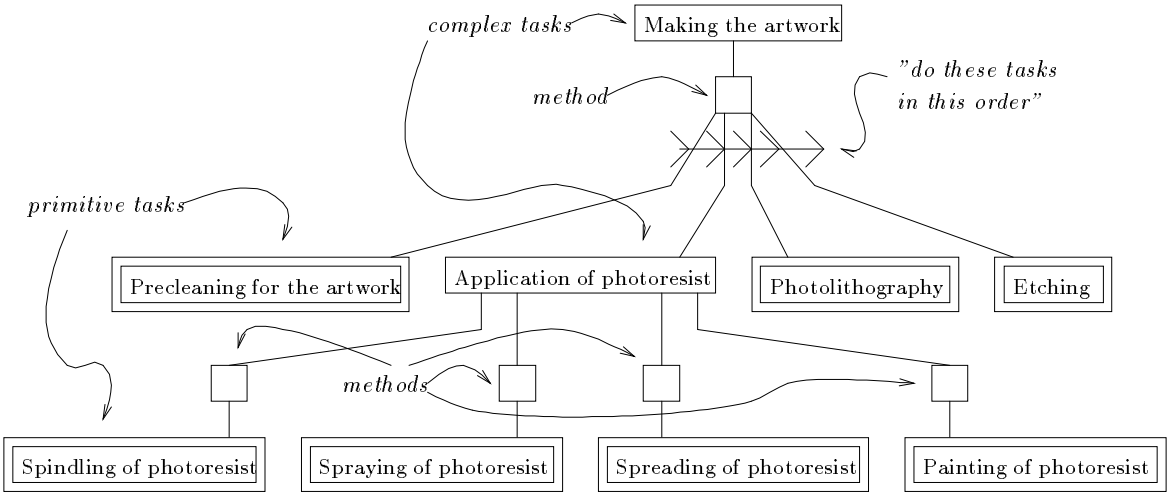

Figure 6 Part of the task network for microwave T/R module manufacture.

some of our other work [27, 28]. In EDAPS, process planning proceeds by taking a complex *task* to be performed and considering various *methods* for accomplishing the task. Each method provides a way to decompose the task into a set of smaller tasks. By applying other methods to decompose these tasks into even smaller tasks, the planner eventually produces a set of primitive operations that it knows how to perform directly.

As an example, one method for making the artwork for the MIC is to do the following series of tasks: precleaning for the artwork, then application of photoresist, then photolithography for the artwork, then etching. There are several alternative methods for applying photoresist: spindling the photoresist, spraying on the photoresist, painting on the photoresist, and spreading out the photoresist from a spinner. This relationship between tasks and methods results in a *task network*, part of which is shown in Figure 6.

This decomposition of tasks into various subtasks is important for process planning for the manufacture of microwave T/R modules for two reasons. First, the decomposition in an HTN naturally corresponds to the decomposition of a MIC into the parts and processes required to manufacture it. Second, the ability to include the complex tasks "make drilling and milling features", "make artwork", "assembly and soldering", and "testing and inspection" in sequence provides a uniform framework that can naturally accommodate both mechanical and electronic manufacturing processes.

Sometimes a particular method can always be used to perform a particular task. For example, because spreading out the photoresist from a spinner is so accurate, this method can always be used to perform the task of applying the photoresist. Sometimes a particular method can only sometimes be used to perform a particular task. For example, because spraying on the photoresist is only somewhat accurate, this method cannot be used to apply the photoresist if a coupler in the artwork has a gap of less than or equal to 10 mils.

Certain tasks, such as precleaning for the artwork, are *primitive*, meaning that they do not break down into any other tasks. Once the complex task of making the entire MIC has been broken down into a series of primitive tasks, a process plan has been created; carrying out the steps of the process plan results in the creation of the MIC.

The planning module constructs a set of process plans, and evaluates them to see which takes the least amount of time. In some cases, it evaluates a set of incomplete process plans

```
Processes:

Opn A   BC/WW   Setup   Runtime   LN    Description
001 A    VMC1    2.00      0.00   01    Orient board
                                  02    Clamp board
                                  03    Establish datum point at
                                        bullseye (0.25, 1.00)
001 B    VMC1    0.10      0.43   01    Install 0.30-diameter drill bit
                                  02    Rough drill at (1.25, -0.50)
                                        to depth 1.00
                                  03    Finish drill at (1.25, -0.50)
                                        to depth 1.00
001 C    VMC1    0.10      0.77   01    Install 0.20-diameter drill bit
                                  02    Rough drill at (0.00, 4.88)
                                        to depth 1.00
                                  [...]
001 T    VMC1    2.20      1.20   01    Total time on VMC1
[...]
004 A    VMC1    2.00      0.00   01    Orient board
                                  02    Clamp board
                                  03    Establish datum point at
                                        bullseye (0.25, 1.00)
004 B    VMC1    0.10      0.34   01    Install 0.15-diameter side-milling tool
                                  02    Rough side-mill pocket at (-0.25, 1.25)
                                        length 0.40, width 0.30, depth 0.50
                                  03    Finish side-mill pocket at (-0.25, 1.25)
                                        length 0.40, width 0.30, depth 0.50
                                  [...]
004 C    VMC1    0.10      1.54   01    Install 0.08-diameter end-milling tool
                                  [...]
004 T    VMC1    2.50      4.87   01    Total time on VMC1
```

Figure 7 Output of EDAPS's planner: a process plan in a standard format, part one.

and discards all but the one which takes the least amount of time. For example, because the method of application for photoresist does not affect the method of application for solder paste, if the quickest method of applying photoresist is spraying it on, then there is no need to generate process plans in which some other method of application is used. If no process plans can manufacture the device—because some manufacturability constraint, such as achievable tolerance, is violated—EDAPS's planner reports the failure and the reason for the failure to the designers.

This generative process planning approach allows us to provide feedback about manufacturability and lead time to the designers, based on actual process plans for the manufacture of the device. Because manufacturing engineers are accustomed to a standard format for the specification of process plans, EDAPS's planner outputs the process plan in this format. See Figure 7 and Figure 8.

```
Opn A   BC/WW   Setup   Runtime   LN    Description
005 A     EC1    0.00     32.29   01    Pre-clean board (scrub and wash)
                                   02    Dry board in oven at 85 deg. F
005 B     EC1   30.00      0.48   01    Setup
                                   02    Spread photoresist
                                         from 18000 RPM spinner
005 C     EC1   30.00      2.00   01    Setup
                                   02    Photolithography of photoresist
                                         using phototool in "real.iges"
005 D     EC1   30.00     20.00   01    Setup
                                   02    Etching of copper
005 T     EC1   90.00     54.77   01    Total time on EC1

006 A     MC1   30.00      4.57   01    Setup
                                   02    Prepare board for soldering
006 B     MC1   30.00      0.29   01    Setup
                                   02    Screenprint solder stop on board
006 C     MC1   30.00      7.50   01    Setup
                                   02    Deposit solder paste at (3.35,1.23)
                                         on board using nozzle
                                   [...]
                                   31    Deposit solder paste at (3.52,4.00)
                                         on board using nozzle
006 D     MC1    0.00      5.71   01    Dry board in oven at 85 deg. F
                                         to solidify solder paste
006 T     MC1   90.00     18.07   01    Total time on MC1
[...]
011 A     TC1    0.00     35.00   01    Perform post-cap testing on board
011 B     TC1    0.00     29.67   01    Perform final inspection of board
011 T     TC1    0.00     64.67   01    Total time on TC1

999 T          319.70    403.37   01    Total time to manufacture
```

Figure 8 Output of the EDAPS's planner: a process plan in a standard format, part two.

6 USING THE SYSTEM

This section describes the interaction between the various modules of the design environment, and the mechanism that integrates these modules into a single toolkit.

Electronic designers, mechanical designers, and manufacturing engineers usually have different requirements for output from the toolkit. For an electronic designer, the integration mechanism must be able to give feedback on the lead times of process plans. It should also inform the designer about mechanical constraints, such as the maximum board temperatures and size constraints on the design. For a mechanical designer, the integration mechanism should automatically generate the shape description of the design. For a manufacturing engineer, process plans are the most important, because they enable

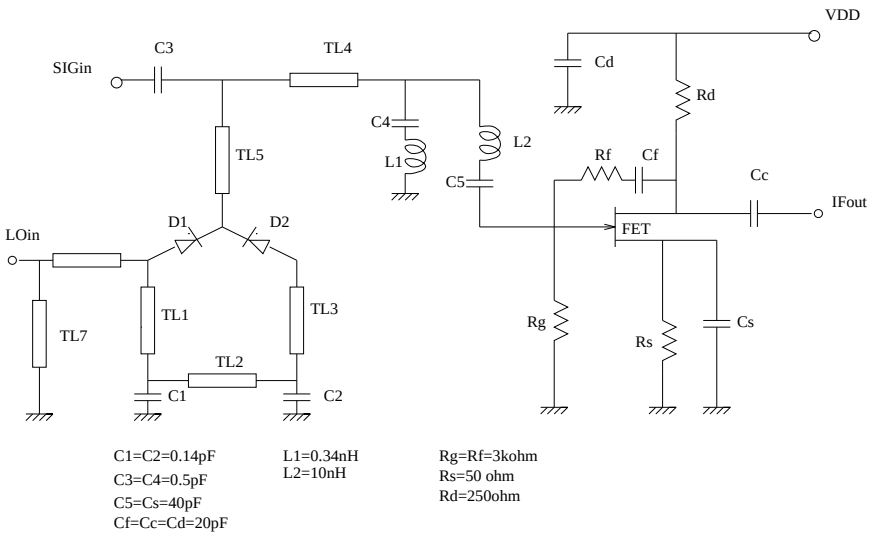

Figure 9 Mixer-IF amplifier schematic circuitry.

the engineer to determine the ease with which the product can be manufactured, and associated costs and lead times.

We provide the mechanism for the exchange of domain-specific product attributes, with the ultimate objective of feeding back plan-based cost, quality and lead times to the designers. The integration, highlighted with an example, is explained below. It describes the steps which will usually be followed in designing a module. Designers can manually change the design during any of the design phases.

Step 1 Schematic Circuit—Circuit Schematic and Circuit Layout Module
For the purpose of illustration, we use the example of a Mixer-IF amplifier circuitry [17] shown in Figure 9. The designers choose the circuit schematic and layout module from the user interface. EEsof's *Libra* package is invoked. The designers generate an initial network of circuitry based on device specifications. The schematic circuit is then simulated, using EEsof's *Touchstone* package. The final values of all component parameters are listed in Figure 9.

Step 2 Artwork Layout—Circuit Layout and Circuit Schematic Module
Assuming satisfactory simulation, then from within Libra, the designers invoke ACADEMY to generate the layout of the circuitry (see Figure 10). Once artwork generation is completed, the system calls an application program that extracts the product information relevant for manufacturing from the design databse, and stores it in C++ classes. Finally, the system translates the layout into an IGES file [14], and exports it to Microstation for substrate designing.

Step 3 Mechanical design—Substrate Design Module
Microstation is then invoked from the user interface. The Microstation kernel reads layout from the IGES file and product information from the C++ classes, and regenerates the artwork as a Microstation design file. Figure 11 illustrates some of the package shapes that will be generated by Microstation.
As can be seen in Figure 11, milled pockets for high-heat dissipating components—such as the diodes and the FET in the example—will be automatically generated from

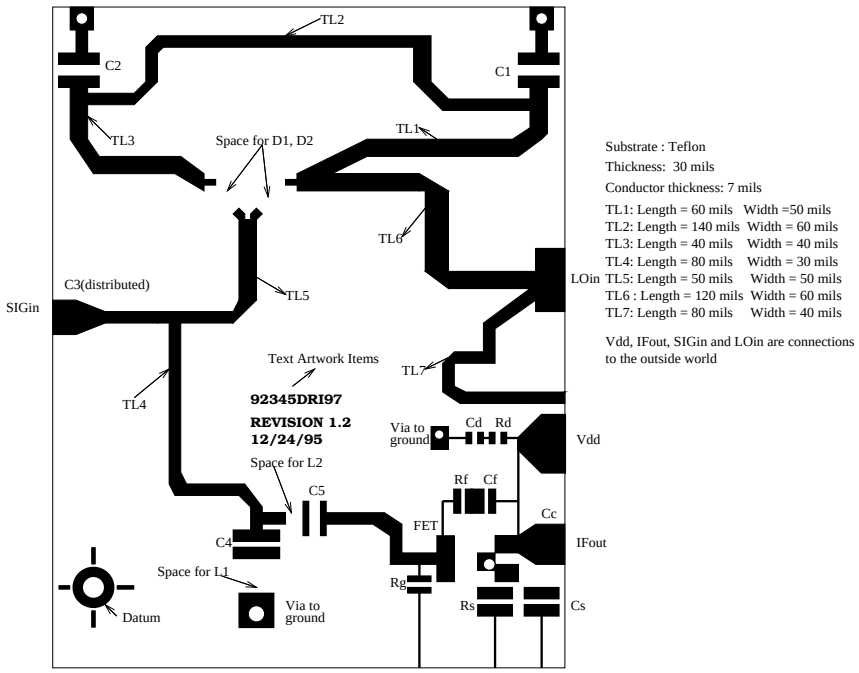

Figure 10 Mixer-IF amplifier circuitry layout.

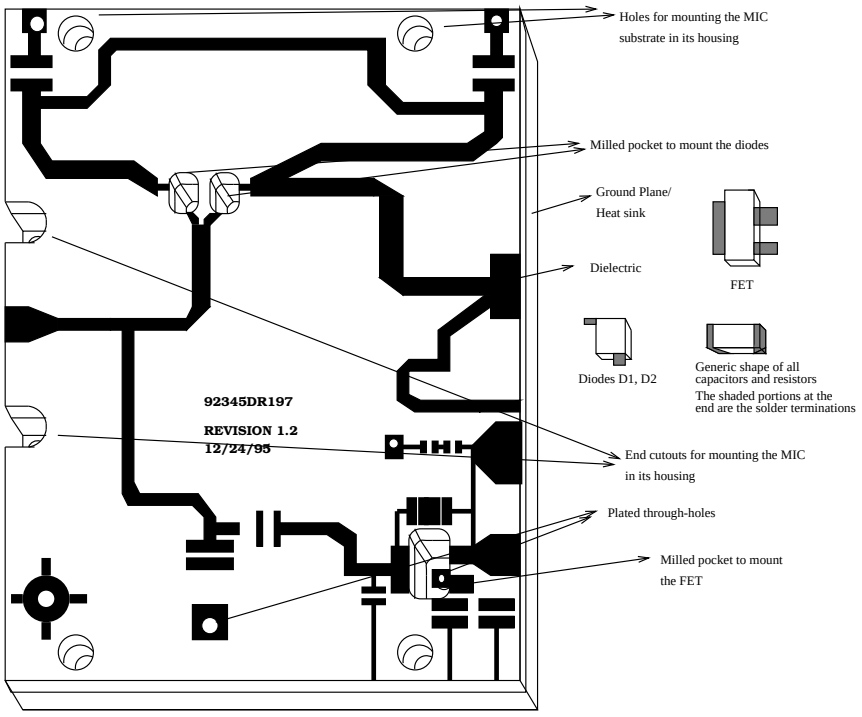

Figure 11 Development of mechanical features on the Mixer-IF amplifier substrate.

the size information of their respective packages. When the mechanical design phase is complete, information about the location, type, and dimensions of all machined features and packaged components are written to a file that is read by the process planner.

Step 4 Process Planner—Process Planning Module

As we have mentioned, EDAPS's planner works by decomposing complex tasks into simpler tasks. The initial task, which decomposes into all other required tasks, is simply called "Make board".

Consider Figure 11. "Make board" decomposes into "Make plated through-holes and features"; "Make artwork"; "Assembly"; and "Testing and inspection". "Make plated through-holes and features" decomposes into "Drill plated through-holes"; "Plate plated through-holes"; and "Make features". "Drill plated through-holes" and "Plate plated through-holes" decompose into primitive tasks which we do not discuss here.

"Make features" is the next task, and because there are features left to be made, it decomposes into "Make a single feature", and "Make features". This "loop" in the task network allows us to decompose a task, such as "Make features", into zero or more subtasks, such as "Make a single feature".

"Make a single feature" decomposes into "Setup and side-mill (the bottom cutout on the left side of the substrate)". "Setup and side-mill (the bottom cutout on the left side of the substrate)" decomposes into "Setup"; "Setup side-milling tool"; and "Side mill". Because the part is not currently set up on the machining center, "Setup" decomposes into "Orient the part"; "Clamp the part"; and "Establish a datum point". All three of these tasks are primitive.

"Setup side-milling tool" is the next task, and because we just started machining, we assume that the correct side-milling tool is not installed on the machining center. Thus, this task decomposes into "Install side-milling tool (of the appropriate size)", which is a primitive task. Assuming tight tolerances, "Side mill" decomposes into "Rough side-mill" and "Finish side-mill", both of which are primitive tasks.

"Make features" continues to decompose until a plan has been created for all five milling features and all thirteen drilling features in the substrate.

The next task of interest is "Make artwork". "Make artwork" decomposes into "Preclean for artwork"; "Apply photoresist"; "Artwork photolithography"; and "Etching". In our planner, all of these tasks but "Apply photoresist" are primitive. "Apply photoresist" has several alternative decompositions: "Spread photoresist from a spinner", or "Spindling the photoresist", or "Spraying the photoresist". "Apply photoresist" does **not** decompose into "Painting on the photoresist" in this case, because painting on the photoresist is not accurate enough for this substrate.

As mentioned before, because the method of application of photoresist does not affect anything else in the plan, EDAPS's planner locally decides which photoresist application method is cheapest in this instance—"Spread photoresist from a spinner", let us say—and keeps only that subtask in the plan.

The rest of the plan is generated in a similar manner, and is output as shown in Figure 7 and Figure 8. The output of EDAPS's planner includes:

- A totally ordered sequence of process specifications that can be used to produce the finished substrate from the materials given;
- Process parameters of all the processes that are required to manufacture the device;
- Estimates of lead times.

The output can be fed back to the designers, with lead-time "hot spots" indicated. The designers may then change the design elements, in order to reduce the lead time.
When the designers and manufacturing engineers are satisfied with the design, the artwork elements will be extracted out of Microstation, and the equivalent IGES file will be generated and sent to ACADEMY. ACADEMY can then export the design file in either IGES format or Gerber format for manufacturing.

7 CONCLUSIONS

In this paper we have described the process planning module used in the EDAPS system. EDAPS is a design and process planning environment whose goal is to integrate mechanical and electronic design tools in a single platform, and to assist the designers in evaluating designs based on the manufacturing plans. The distinct advantage of such an approach is the ability to evaluate designs from the point of view of the designers and the manufacturers. EDAPS thus highlights a concurrent engineering approach that we have taken to reduce the lead times, and to improve the quality in electronic manufacturing.

The process planning module of EDAPS has been completed, although its knowledge base is still being tested and fine-tuned. Parts of the rest of EDAPS are still under development. To date, we have completed the routines to extract and store relevant manufacturing information from electronic designs and the routines that build the manufacturing features. Work that remains to be done includes building the routines to generate shape representations of packaged component features.

7.1 Lessons Learned So Far

Integration of Electrical and Mechanical Design. In order to avoid developing a large monolithic system from scratch, we decided to use existing commercial systems for electrical and mechanical design. In addition to providing ways for the electrical and mechanical design systems to exchange information with each other, this required extending the electronic design system to keep track of some of the information needed for mechanical design so that this information will not be lost when users change the electrical design, and similarly extending the mechanical design system to keep track of some of the information needed for the electronic design.

The disadvantage of using existing commercial tools in this way is that it may limit the interaction between the electronic design system and the mechanical CAD system, and that in any case translating and transferring information from one system to another takes time and work. (In our system, because our feedback was based on the process plan for manufacturing, we didn't have to translate and transfer much information between the electronic design system and the mechanical CAD system to be able to feed back information about cost and lead time. EEsof's built-in features automatically handled manufacturability feedback.) However, the use of existing commercial tools allows companies to keep legacy systems in place; in addition, designers can change their electronic design system without changing their mechanical CAD system, or vice versa.

Process Planning and Manufacturability Analysis. Hierarchical task-network planning appears to be an ideal approach for generative process planning for microwave mod-

ules. The decomposition in an HTN naturally corresponds to the decomposition of a microwave integrated circuit into the parts and processes required to manufacture it, and HTN's provide a unified framework that accommodates both electronic and mechanical manufacturing processes.

Although researchers have had great difficulty in developing generative process planners that produce realistic process plans for complex mechanical parts, generative process planning can be more easily applied to microwave T/R modules. In microwave T/R modules, the interactions among mechanical features are much fewer and simpler than the complex geometric interactions that can occur in complex mechanical parts as described in [10, 20].

In many AI planning systems, the way of representing information about the world is as a collection of *logical atoms* (elementary expressions in first-order logic). For basic research on AI planning, this approach has a number of benefits. However, in applying HTN planning to our problem domain, we found it important to represent the data in such a way as to facilitate integrating the planner with the other EDAPS modules. For example, in order to communicate with the Microstation modeler, the planner needs to access complex geometric information that would be difficult to represent or manipulate as sets of logical atoms. Thus, we allowed the representation to consist of arbitrary data structures as appropriate for the task at hand. This let us represent the data in a way that was often much simpler than the corresponding logical atoms would be.

Task-Network Decomposition and Total Ordering. HTN planning has long been thought to have better potential applicability to practical planning problems than other AI planning methods [32], and our experience confirms this opinion. We found HTN planning to be quite natural in process planning for complex electro-mechanical devices, because the planning hierarchy derives naturally from the part-whole hierarchy of the device itself.

However, even though EDAPS's process planning module is an HTN planner, it differs from almost all other HTN planners in that it is a total-order planner. Because its task networks are totally ordered, so are all the plans that it generates. Furthermore, it expands tasks in the order in which they will be achieved: given a sequence of tasks to accomplish, it will always expand whichever task needs to be performed first.

However, we did *not* make use of another AI planning technique used in most current AI planning systems—the use of "partial-order planning", in which the order in which a planner can construct plans for the goals it is trying to achieve is a different order from the order in which it intends to execute those plans. For example, if one wants to fly to another continent, a partial-order planner might think about what flight to take before bothering to develop a plan for getting from home to the airport. This way, the planner can constrain its search space by making some "important" or "bottleneck" decision before committing to other less-important steps. However, planning for a task that will come later in a plan before one has planned everything that will come before them also incurs a drawback: when one is planning for the later task, one cannot know what the task's input state will be, because one does not know what sequence of steps will produce this input state. This fundamental source of uncertainty can make the planning mechanism much more complex than it would be otherwise.

In developing EDAPS's process planner, we felt that even though situations might occur where it might be useful to plan for a later task before planning for an earlier task, such situations would not occur often enough to make it worth the trouble to develop the

complex planning mechanisms and data structures that this would require. Thus EDAPS's process planner may be described as a "total-order HTN planner."

Our experience suggests that total-order HTN planning approach is a promising approach in a number of application domains. Not only does it appear to work well in process planning for microwave T/R modules—but as described in [27, 28], the same approach (and some of the same code!) also works quite well in another very different application domain: declarer play in the game of contract bridge.

In both of our application domains, planning the tasks in the order that they are to be executed makes it easy for us to use data representations much more flexible than those normally used in AI planning. This makes it much easier to interface the planner to external information sources, and greatly facilitates the task of creating the planner's knowledge base. Both of these activities are crucial for the development of successful planners in realistic application domains.

Plan Explanation. Our generative process planning approach allowed us to provide feedback about manufacturability and lead time to the designers, based on actual process plans for the manufacture of the device. Because manufacturing engineers are accustomed to a standard format for the specification of process plans, EDAPS's planner needed to output the process plan in this format. Adhering to this format required a lot of work.

While this *plan explanation* may seem a small detail—certainly no advanced AI techniques were required—it is a crucial feature of EDAPS's planner. Without EDAPS's plan explanation, its plans would be useless. The issue of plan explanation appears to be important, and we are unaware of any formal approaches to plan explanation.

7.2 Future Work

In real life situations, designers never obtain a truly optimum design. A design that is optimal with respect to cost may have poor yields associated with it. In such cases, trade-offs have to be done to attain a design solution that is "somewhat optimal" with respect to all the decision variables.

We plan to incorporate a trade-off analysis module that gives the designers a clearer picture of all the cost versus quality trade-off issues that are involved in each design. To do such trade-off analysis, models to predict yields and costs are needed. To estimate the costs, several formulae are available from standard process handbooks. However, yields are more difficult to predict. The simplest yield model associates a historically determined yield value with each component. In that case, component design features will have quality as an additional attribute. The fundamental assumption with this model is that yields are determined solely by components, and not by the processes involved in the manufacture nor by the designs in which the components appear.

In fact, processes, components, and board design characteristics all determine the yield of the microwave T/R modules. Ball and others [2] consider such interactions between processes and parts, and solve the trade-off analysis as an integer-programming problem. However, they require individual process-component yield values as inputs for their models. For new designs, such as the ones we are considering, it is hard to predict such process-component yield values without having subjected the product to several runs in production lines. In the future, we will do further research to determine the yield model most suitable for our application.

8 REFERENCES

[1] *ACIS Geometric Modeler* (1993) Spatial Technology, Inc., Boulder, Colorado.

[2] Ball, M. O., Baras, J. S., Bashyam, S., Karne, R. K., and Trichur, V.(1995) On the selection of parts and processes during design of printed circuit board assemblies, in *Proceedings of the INRIA/IEEE Symposium on Emerging Technologies and Factory Automation* **3**, 241–9, IEEE Computer Society Press, Los Alamitos, California.

[3] Brindley, K.(1990) *Newnes electronics assembly handbook.* Heinemann Newnes, Oxford, England.

[4] Candadai, A., Herrmann, J.W., Minis, I., and Ramachandran, V.(1994) Product and process models for microwave modules, in *Proceedings of the ASME Winter Annual Meeting*, Chicago, Illinois, December 1994.

[5] Chenu, J. P. and Müller, H.(1989) Manufacture of Microwave Telecommunication Equipment. *Electrical Communication* **63:2**, 159–167.

[6] *EEsof Series IV version 4.*(1992) EEsof Inc., Westlake Village, California.

[7] Erol, K., Hendler, J., and Nau, D. S.(1994) HTN planning: complexity and expressivity, in *Proceedings of the Twelfth National Conference on Artificial Intelligence*, 1123–1128, AAAI, Menlo Park, California.

[8] Feldmann, K. and Franke, J.(1993) Computer-Aided Planning Systems for Integrated Electronic and Mechanical Design. *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, **16:4**, June 1993, 377–383.

[9] Geelink, R., Salomons, O., van Slooten, F., van Houten, F., and Kals, H.(1995) Unified feature definition for feature based design and feature based manufacturing, in *Computers in Engineering 1995* (ed. A. Busnaina), 517–533, American Society of Mechanical Engineers, New York.

[10] Gupta, S. K. and Nau, D. S.(1995) A systematic approach for analyzing the manufacturability of machined parts. *Computer Aided Design* **27:5**, 343-342.

[11] Harhalakis, G.; Kinsey, A.; Minis, I. and Rathbun, H.(1992) Automated Group Technology Code Generation Using PDES, in *Proceedings of the Third International Conference on Computer Integrated Manufacturing*, Rensselaer Ploytechnic Institute, Troy, New York.

[12] Hebbar, K., Smith, S. J. J., Minis, I. and D. Nau.(1996) Plan-Based Evaluation of Designs for Microwave Modules. *Proceedings of the 1996 ASME Design Technical Conference*, to appear.

[13] Hoffmann, R. K.(1987) *Handbook of Microwave Integrated Circuits.* Artech House, Norwood, Massachusetts.

[14] *The Initial Graphics Exchange Specification (IGES) Version 5.1* (1991) IGES/PDES Organization, Gaithersburg, Maryland.

[15] Ishii, K.(1993) Modeling of concurrent engineering design, in *Concurrent Engineering: Automation, Tools and Techniques* (ed. Andrew Kusiak), pp 19–39, John Wiley & Sons, Inc.

[16] Jakiela, M. and Papalambros, P.(1989) Design and implementation of a prototype intelligent CAD system. *ASME Journal of Mechanisms, Transmissions and Automation in Design*, **111:2**, 252258.

[17] Konishi, Y.(1991) *Microwave Integrated Circuits.* Marcel Dekker, New York, New York.

[18] Liau, J., S. and Young, R. E.(1993) A process planning and concurrent engineering system for PCBs. *Manufacturing Review* **6:1**, March 1993, 25–39.
[19] *Microstation Version 5.*(1995) Bentley Systems, Inc., Exton, Pennsylvania.
[20] D. S. Nau, S. K. Gupta, and W. C. Regli.(1995) AI planning versus manufacturing-operation planning: a case study, in *Proceedings of the 14th International Joint Conference on Artificial Intelligence*, 1670–1676, Morgan Kaufmann, San Mateo, California.
[21] O'Grady, P., Young, R. E., Greef, A., and Smith, L.(1991) An advice system for concurrent engineering. *International Journal of Computer Integrated Manufacturing* **4:2**, 63–70.
[22] Ousterhout, J. K.(1994) *Tcl and the Tk Toolkit.* Addison-Wesley, Reading, Massachusetts.
[23] Sandborn, P.(1992) A software tool for technology tradeoff evaluation in multichip packaging, in *11th IEEE/CHMT International Electronic Manufacturing Technology Symposium*, 337341.
[24] Sander, K. F.(1987) *Microwave Components and Systems.* Addison-Wesley, Reading, Massachusetts.
[25] Sanii, E. T. and Liau, J. S.(1993) An expert process planning system for electronics PCB assembly. *Computers in Electrical Engineering* **19:2**, 113–127.
[26] Shah, J., Mantyla, M., and Nau, D.S.(1994) in *Advances in Feature Based Manufacturing*, Elsevier/North Holland.
[27] Smith, S. J. J., Nau, D. S., and Throop, T.(1996) Total-order multi-agent task-network planning for contract bridge, in *Proceedings of AAAI-96*, to appear.
[28] Smith, S. J. J., Nau, D. S., and Throop, T.(1996) A planning approach to declarer play in bridge. *Computational Intelligence*, **12:1**, February 1996, 106–130.
[29] Toye, G., Cutkosky, M. R., Leifer, L. F., Tenenbaum, T. M., and Glicksman, J.(1994) SHARE: A Methodology and Environment for Collaborative Product Development. *The International Journal of Intelligent and Cooperative Information Systems*, **3:2**, June 1994, pp. 129-53.
[30] Trinogga, L. A., Kaizhou, G., and Hunter, I. C.(1991) *Practical Microstrip Design.* Ellis Horwood, Chichester, UK.
[31] Whitney, D. E., Nevins, J. L., De Fazio, T. L., and Gustavson, R.(1993) Problems and Issues in Design and Manufacture of Complex Electro-mechanical Systems. *C S Draper Laboratory Report*, R-2577, MIT, December 1993.
[32] Wilkins, D. E.(1988) *Practical Planning.* Morgan Kaufmann, San Mateo, California.
[33] Yang, Q.(1990) Formalizing planning knowledge for hierarchical planning. *Computational Intelligence* **6**, 12–24.

9 AUTHOR BIOGRAPHIES

9.1 Stephen J. J. Smith

Stephen J. J. Smith is an assistant professor at Hood College in Frederick, Maryland, in the Department of Mathematics and Computer Science. His research interests include AI planning, search, game-playing, reasoning with uncertainty, and computer-integrated design

and manufacturing (for recent papers, see <http://www.cs.umd.edu/users/sjsmith>). He expects to receive his Ph.D. from the University of Maryland at College Park in December 1996, where he was an AT&T graduate fellow. His dissertation is entitled "Task-Network Planning for Bridge and for Microwave Module Manufacture".

9.2 Kiran Hebbar

Kiran Hebbar is a graduate student at the University of Maryland, in the Department of Mechanical Engineering and the Institute for Systems Research. His research interests are in the areas of computer-integrated design and manufacturing, and electronics manufacturing. Mr. Hebbar is the recipient of the University of Maryland's graduate school fellowship for 1994-96. He graduated with an undergraduate degree in mechanical engineering from the Indian Institute of Technology, Delhi, India in 1994.

9.3 Dana Nau

Dana Nau is a professor at the University of Maryland, in the Department of Computer Science and the Institute for Systems Research. His research interests include AI planning and searching, and computer-integrated design and manufacturing. Dr. Nau received his Ph.D. from Duke University in 1979, where he was an NSF graduate fellow. He has received an NSF Presidential Young Investigator award, the ISR Outstanding Systems Engineering Faculty award, and several "best paper" awards. He has more than 150 technical publications; for recent papers see <http://www.cs.umd.edu/users/nau>. He is a Fellow of the American Association for Artificial Intelligence (AAAI).

9.4 Ioannis Minis

Ioannis Minis is an associate professor at the University of Maryland, in the Department of Mechanical Engineering and the Institute for Systems Research. His research interests include production systems, distributed manufacturing, concurrent engineering, and machining dynamics and control. He has authored over 60 technical publications. He received his Ph.D. in mechanical engineering from the University of Maryland in 1988. He is the recipient of the 1993 Earl E. Walker Outstanding Young Manufacturing Engineer Award of the Society of Manufacturing Engineers. He received the best paper award in the area of Engineering Database Management at the 1992 ASME International Conference on Computers in Engineering.

10 ACKNOWLEDGEMENT AND DISCLAIMER

This work was supported in part by ONR grant N000149610888, by the National Science Foundation under Grants NSF EEC 94-02384, IRI-9306580, and DDM-9201779, and by in-kind contributions from Spatial Technologies and Bentley Systems. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the authors and do not necessarily reflect the views of the funders.